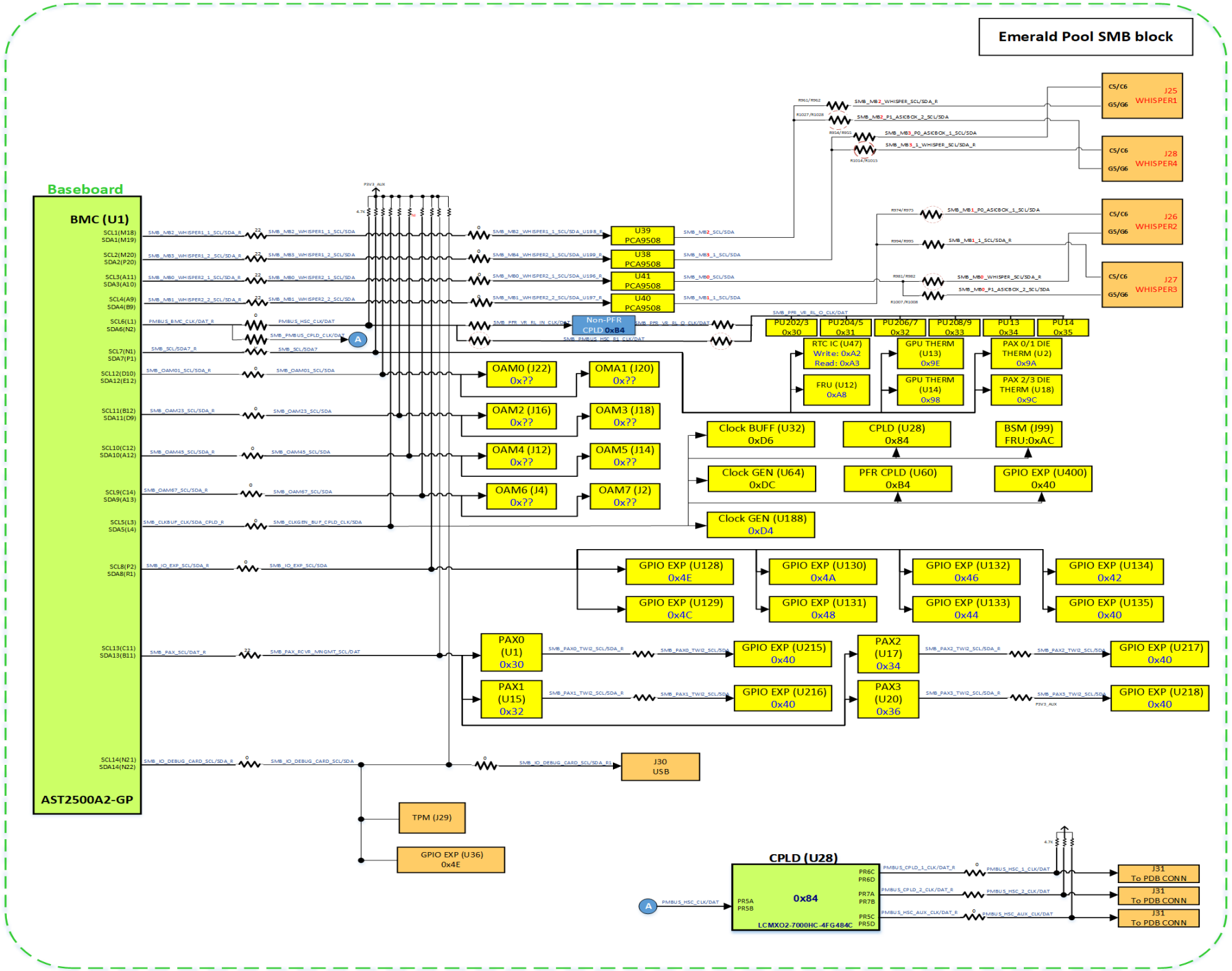
Emerald Pools Baseboard

PCB REV:
PCBA REV:
FAB:
SCH Rev:
LAST UPDATE:

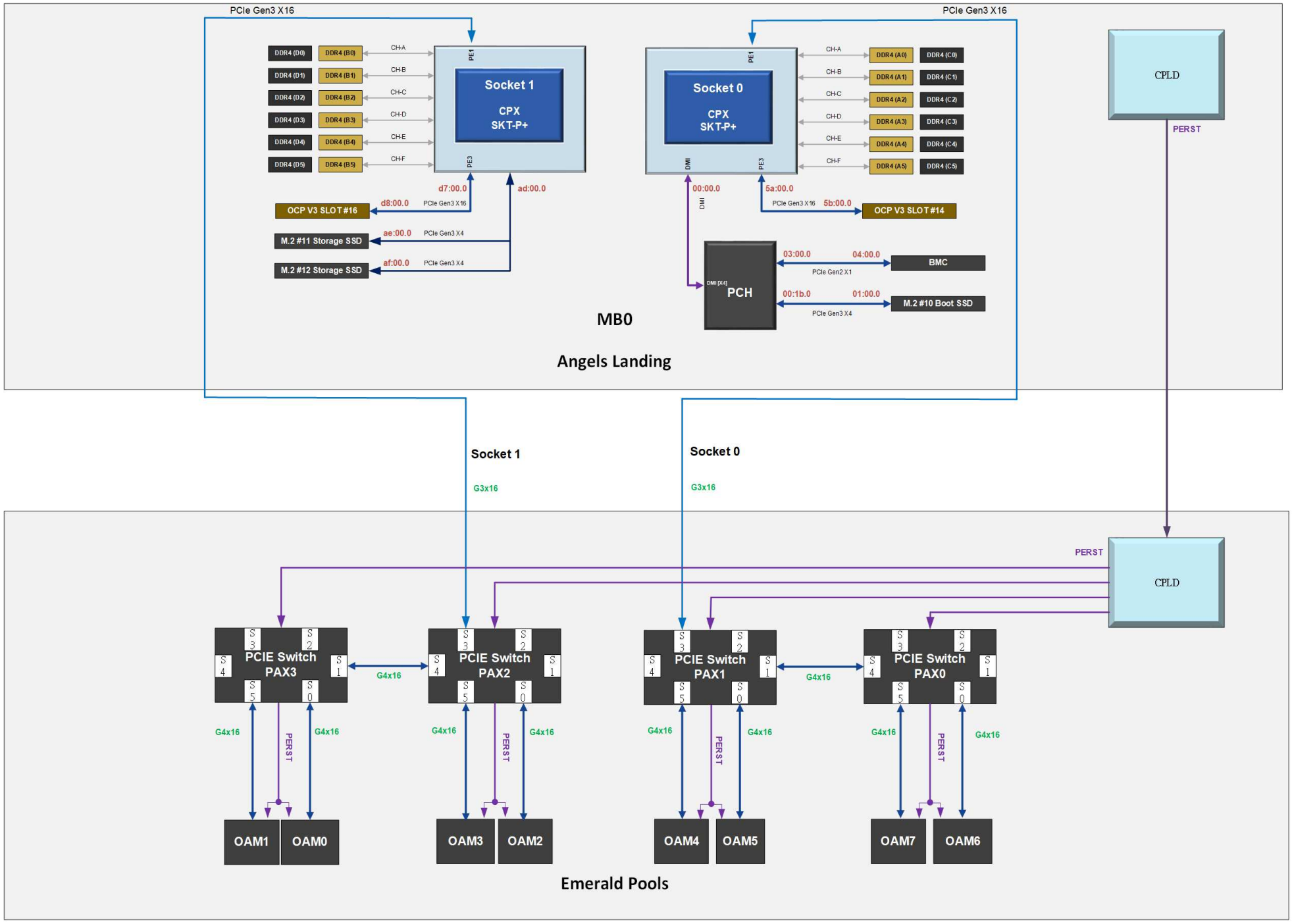
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081 MODULE PWRGD
082 UART TO USB
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086 LEVEL SHIFT(2/2)
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088 BMC_01
089 BMC_02
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092 BMC_HW_STRAPPING_1
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094 BMC_DDRIII_IV_SDRAM
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098 BLANK
099 M.2 CONNECTOR
100 PFR CPLD(1/2)
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103 CPLD (1/4)
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107 WHISPER_CONN1(1/2)
108 WHISPER_CONN1(2/2)
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119 USB DEBUG
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122 USB_OC_PROTECT & USB MUX
123 PWR_BUTTON
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125 I2C_RTC_IC
126 BMC&CPLD DEBUG HEADER
127 SYSTEM STATUS LED CIRIUIT
128 TPM
129 ISOLATOIN_TEST_ASIC0
130 ISOLATOIN_TEST_ASIC1
131 ISOLATOIN_TEST_ASIC2
132 ISOLATOIN_TEST_ASIC3
133 ISOLATOIN_TEST_ASIC4
134 ISOLATOIN_TEST_ASIC5
135 ISOLATOIN_TEST_ASIC6
136 ISOLATOIN_TEST_ASIC7
137 THERMTRIP
138 P3V3 POWER SWITCH
139 VR_P0V8_VDD0
140 VR_P0V8_VDD1
141 VR_P0V8_VDD2
142 VR_P0V8_VDD3
143 VR_P1V0_AVD0_1
144 VR_P1V0_AVD2_3
145 VR_P1V8_VDD0_1_2_3
146 VR_P5V_STBY
147 VR_P3V3_STBY
148 VR_P2V5_AUX
149 VR_P1V2_AUX_P1V15_AUX
150 VR_CPLD_VREFF
151 TDR
152 DELTA_L
153 POWER GOOD LED
154 SCREW HOLE
155 DUMMY SYMBOL

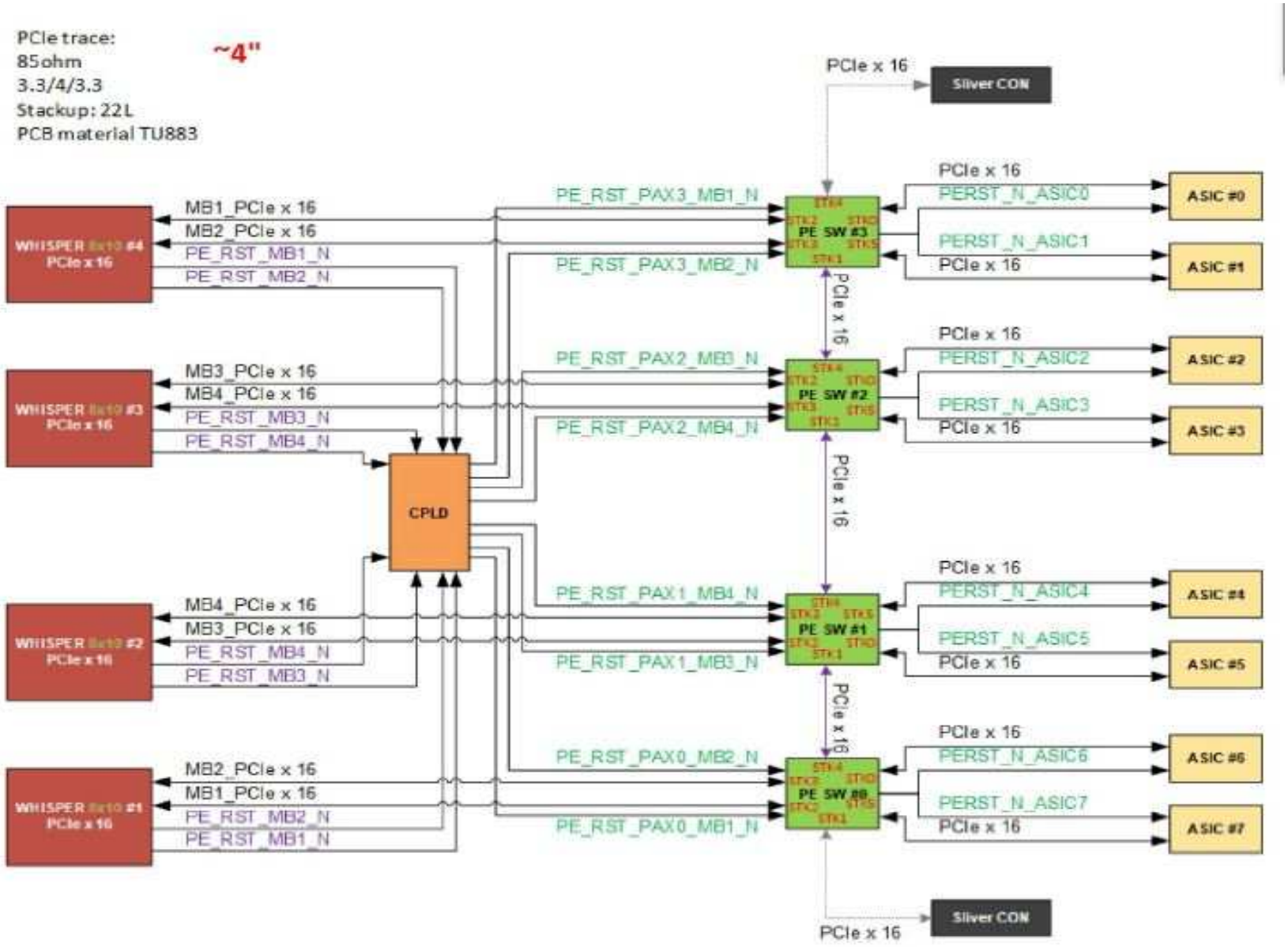


I2C Topology

Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
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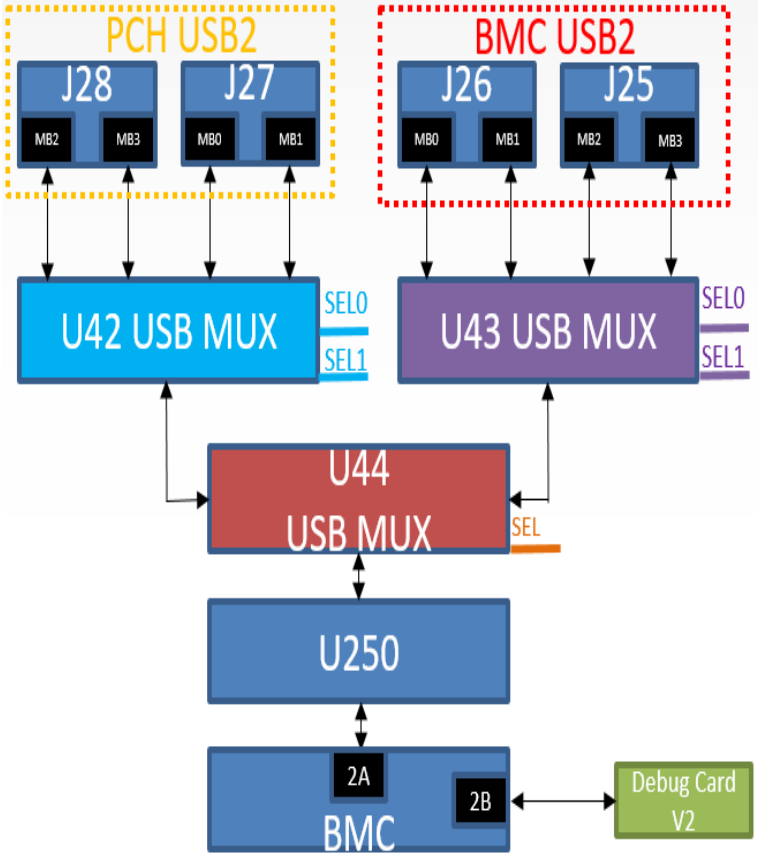
SYSTEM PCIE TOPOLOGY



Baseboard_PCIE_Topology

Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
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EP USB Topology



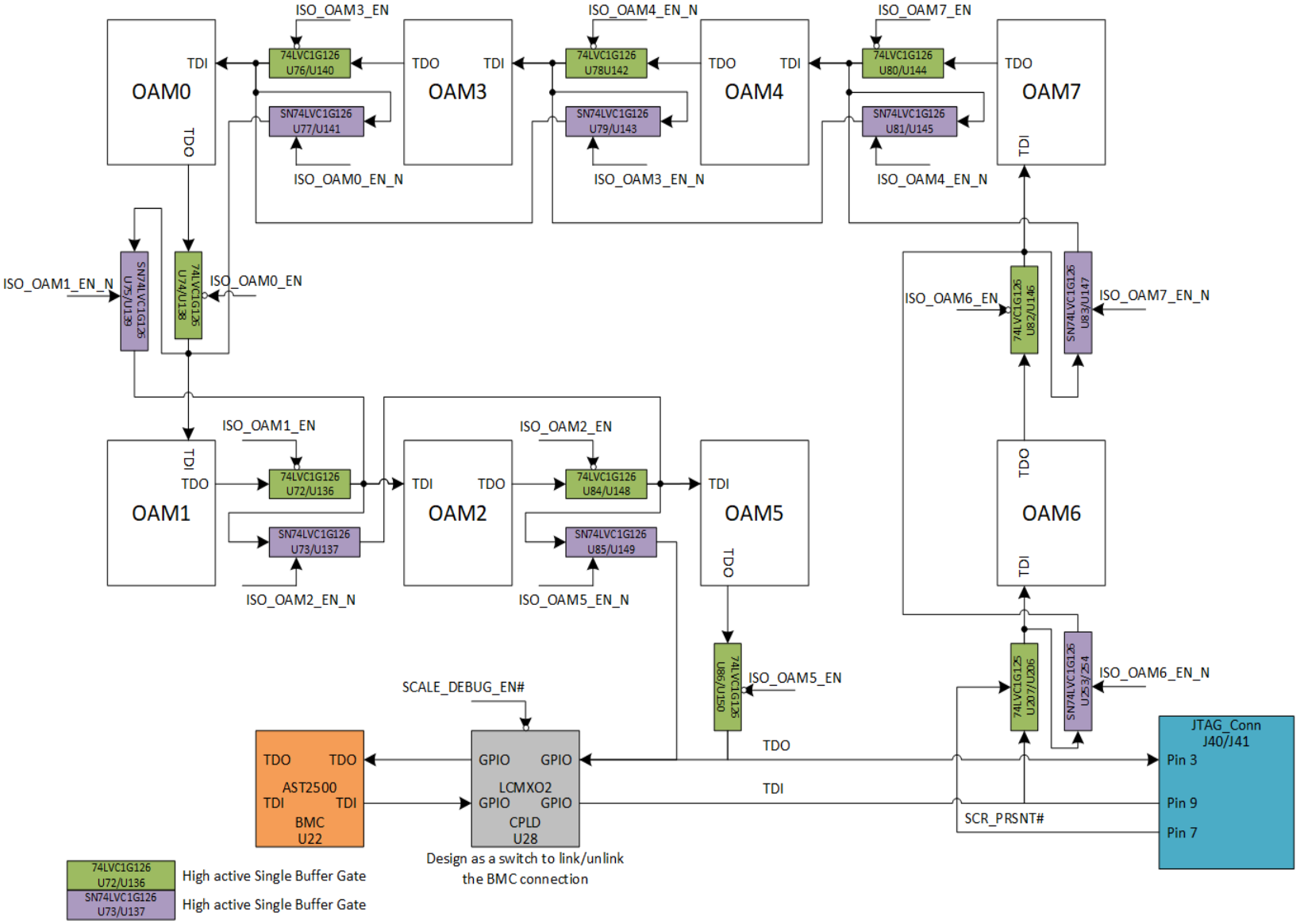
Signal		USB2_SEL0_U43	USB2_SEL1_U43
BMC	MB3	L	L
	MB2	H	L
	MB1	L	H
	MB0	H	H
Signal		USB2_SEL0_U42	USB2_SEL1_U42
PCH	MB3	L	L
	MB2	H	L
	MB1	L	H
	MB0	H	H
Signal		SEL_USB_MUX	
BMC End Piont	BMC	L	
	PCH	H	

USB TOPOLOGY

STACKUP																	
						Target Z (ohms) - MicroStrip	50	Breakout	85		90		95		Breakout	
						Target Z (ohms) - StripLine	50		85		90		95			
						Z tolerance	±10%		±10%		±10%		±10%			
						Z Type	Single	Single	Differential		Differential		Differential		Differential	
Layer#	Material	Description	Copper Weight (oz)	Thickness (mil)	Tolerance (mil)	Glass Fabric	Er	Width	Width	Width	Space	Width	Space	Width	Space	Width	Space
		Soldermask		0.60			3.8										
1		TOP	0.5+plating	1.95				5.3	3.5	5.85	7.05	5.15	7.05	4.55	7.45	3.5	4
	EM-890K	PP		2.70	±0.709	1078x1	2.9										
2		GND	1 (HVLP)	1.30													
	EM-890K	CORE		4.00	±0.709	1035x2	3										
3		IN1	1 (HVLP)	1.30				4.6	3.5	5.7	6.1	4.9	5.8	4.5	6	3.5	4
	EM-890K	PP		4.70	±0.984	2116x1	3										
4		GND1	1 (HVLP)	1.30													
	EM-890K	CORE		4.00	±0.709	1035x2	3										
5		IN2	1 (HVLP)	1.30				4.6	3.5	5.7	6.1	4.9	5.8	4.5	6	3.5	4
	EM-890K	PP		4.70	±0.984	2116x1	3										
6		GND2	1 (HVLP)	1.30													
	EM-890K	CORE		4.00	±0.709	1035x2	3										
7		IN3	1 (HVLP)	1.30				4.6	3.5	5.7	6.1	4.9	5.8	4.5	6	3.5	4
	EM-890K	PP		4.70	±0.984	2116x1	3										
8		GND3	1 (HVLP)	1.30													
	EM-890K	CORE		4.00	±0.709	1035x2	3										
9		IN4	1 (HVLP)	1.30				4.6	3.5	5.7	6.1	4.9	5.8	4.5	6	3.5	4
	EM-890K	PP		4.70	±0.984	2116x1	3										
10		GND4	1 (HVLP)	1.30													
	EM-890K	CORE		4.00	±0.709	1035x2	3										
11		VCC	2 (RTF)	2.60													
	EM-890K	PP		5.00	±0.984	1078x2	3										
12		VCC	2 (RTF)	2.60													
	EM-890K	CORE		4.00	±0.709	1035x2	3										
13		GND5	1 (HVLP)	1.30													
	EM-890K	PP		4.70	±0.984	2116x1	3										
14		IN5	1 (HVLP)	1.30				4.6	3.5	5.7	6.1	4.9	5.8	4.5	6	3.5	4
	EM-890K	CORE		4.00	±0.709	1035x2	3										
15		GND6	1 (HVLP)	1.30													
	EM-890K	PP		4.70	±0.984	2116x1	3										
16		IN6	1 (HVLP)	1.30				4.6	3.5	5.7	6.1	4.9	5.8	4.5	6	3.5	4
	EM-890K	CORE		4.00	±0.709	1035x2	3										
17		GND7	1 (HVLP)	1.30													
	EM-890K	PP		4.70	±0.984	2116x1	3										
18		IN7	1 (HVLP)	1.30				4.6	3.5	5.7	6.1	4.9	5.8	4.5	6	3.5	4
	EM-890K	CORE		4.00	±0.709	1035x2	3										
19		GND8	1 (HVLP)	1.30													
	EM-890K	PP		4.70	±0.984	2116x1	3										
20		IN8	1 (HVLP)	1.30				4.6	3.5	5.7	6.1	4.9	5.8	4.5	6	3.5	4
	EM-890K	CORE		4.00	±0.709	1035x2	3										
21		GND9	1 (HVLP)	1.30													
	EM-890K	PP		2.70	±0.709	1078x1	2.9										
22		BOTTOM	0.5+plating	1.95				5.3	3.5	5.85	7.05	5.15	7.05	4.55	7.45	3.5	4
		Soldermask		0.60			3.8										
			Total	121.70	±10%												

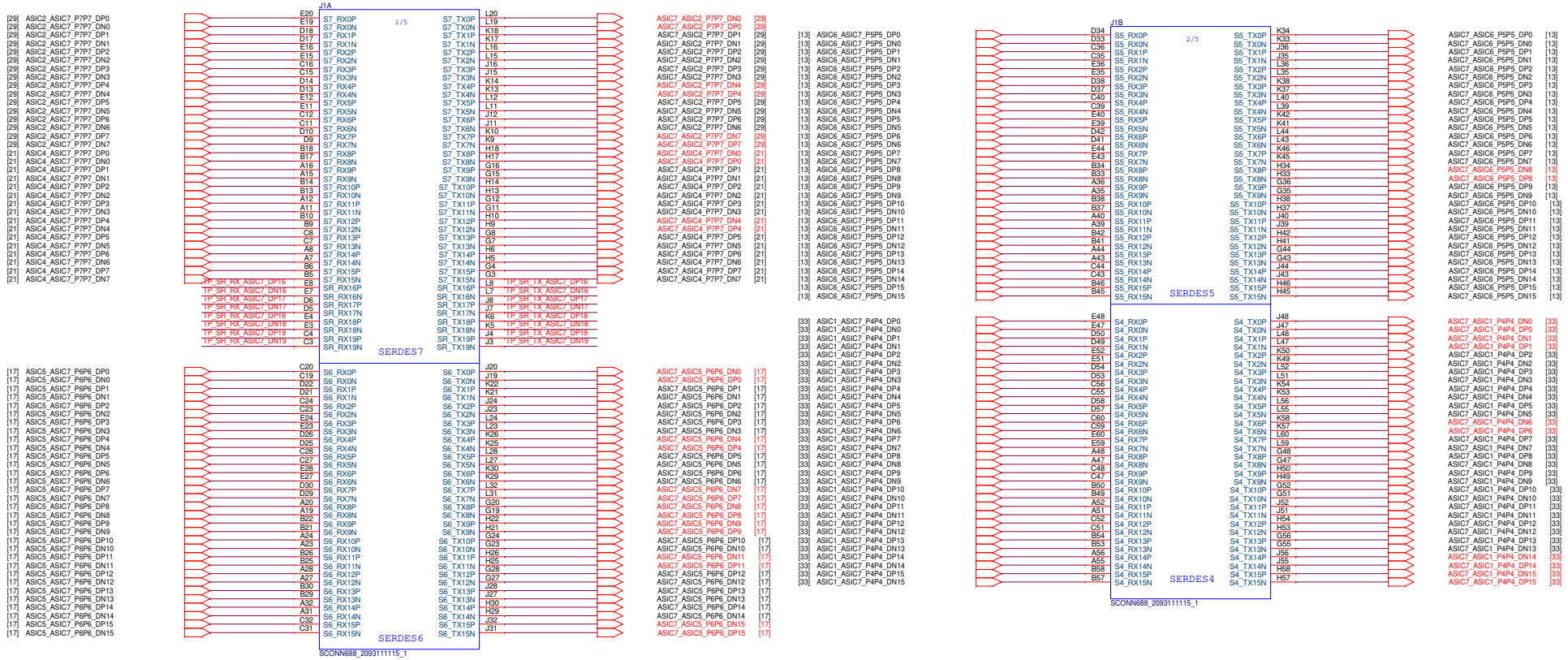
STACKUP

Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
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JTAG TOPOLOGY

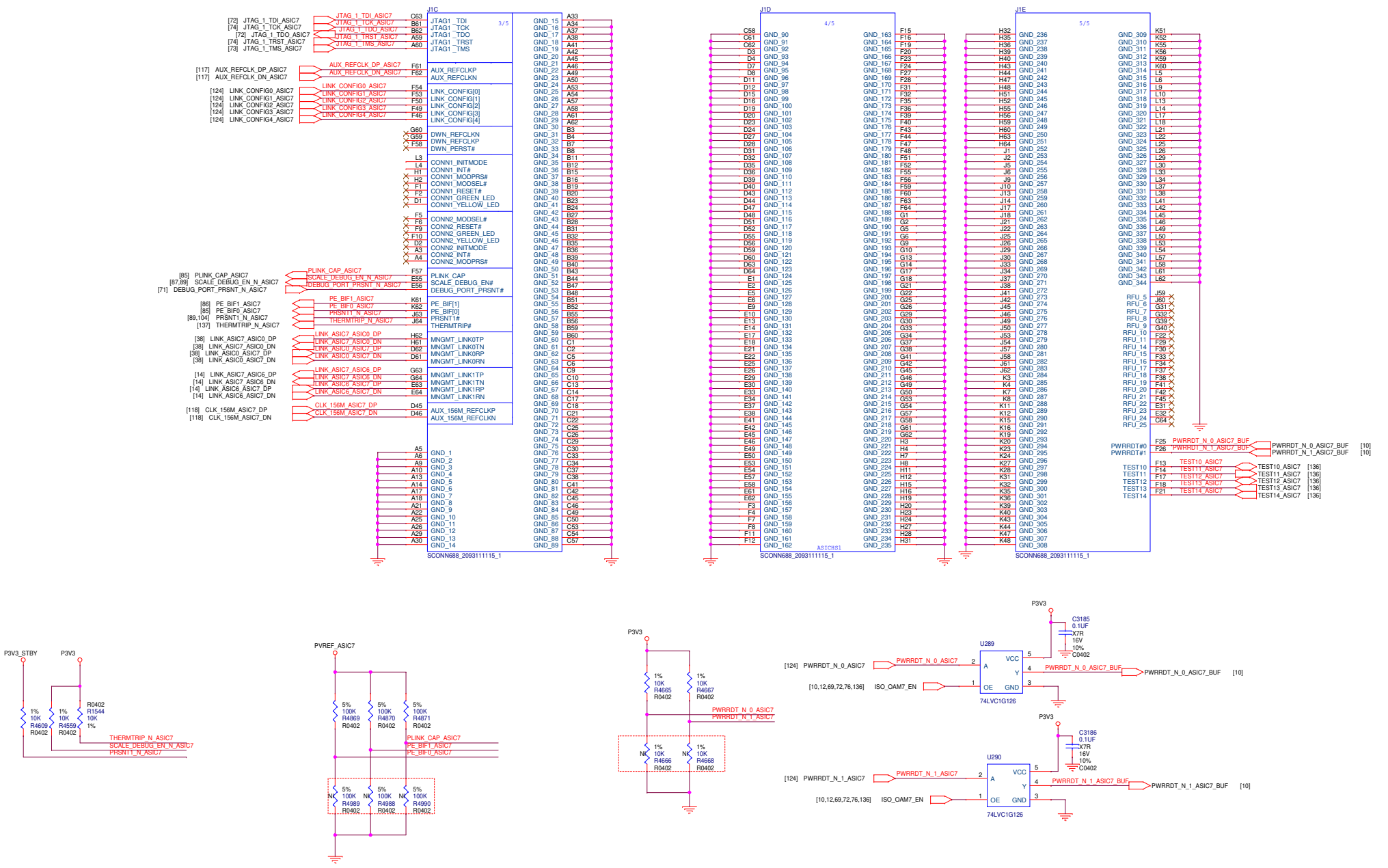
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		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 8 of 155



NOTE:Polarity reversal is marked in red

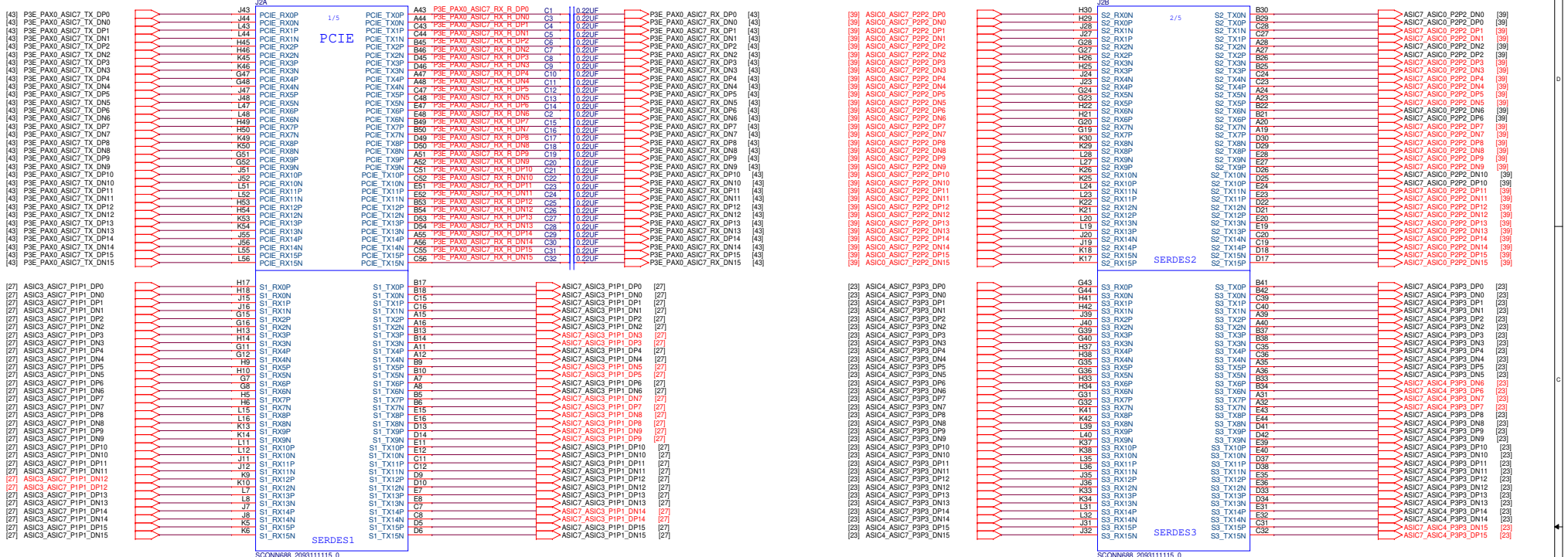
ASIC7_SERDES

Quanta	Department: CCBU	Designer: <Designer>	Project: <project_name>	Doc Number: EP_BASEBOARD_OCP
		Reviewer: <Reviewer>	Size	Date: Tuesday, January 18, 2022
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ASIC7_SERDES_SIDEBAND

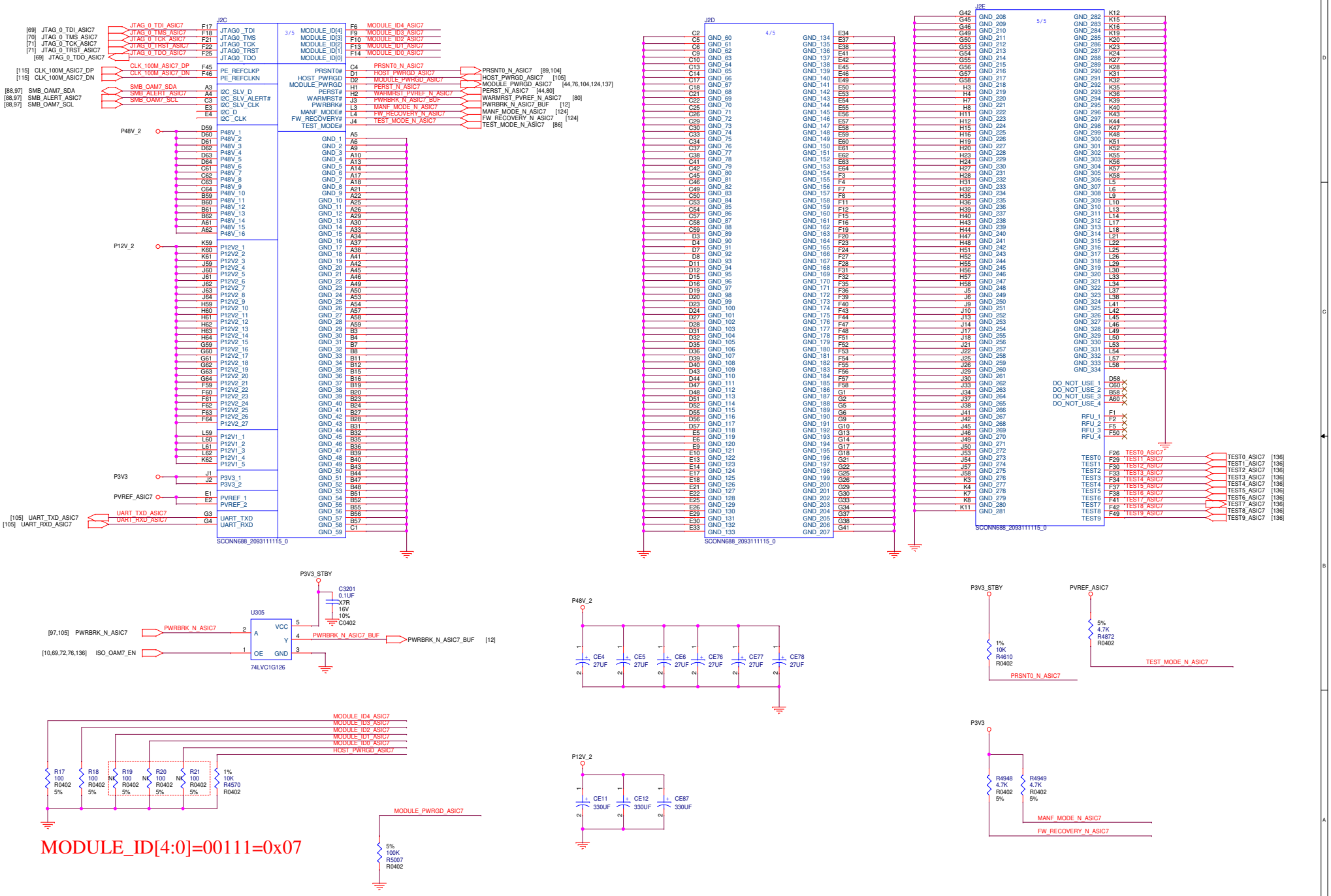
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		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 10 of 155



NOTE:Polarity reversal is marked in red

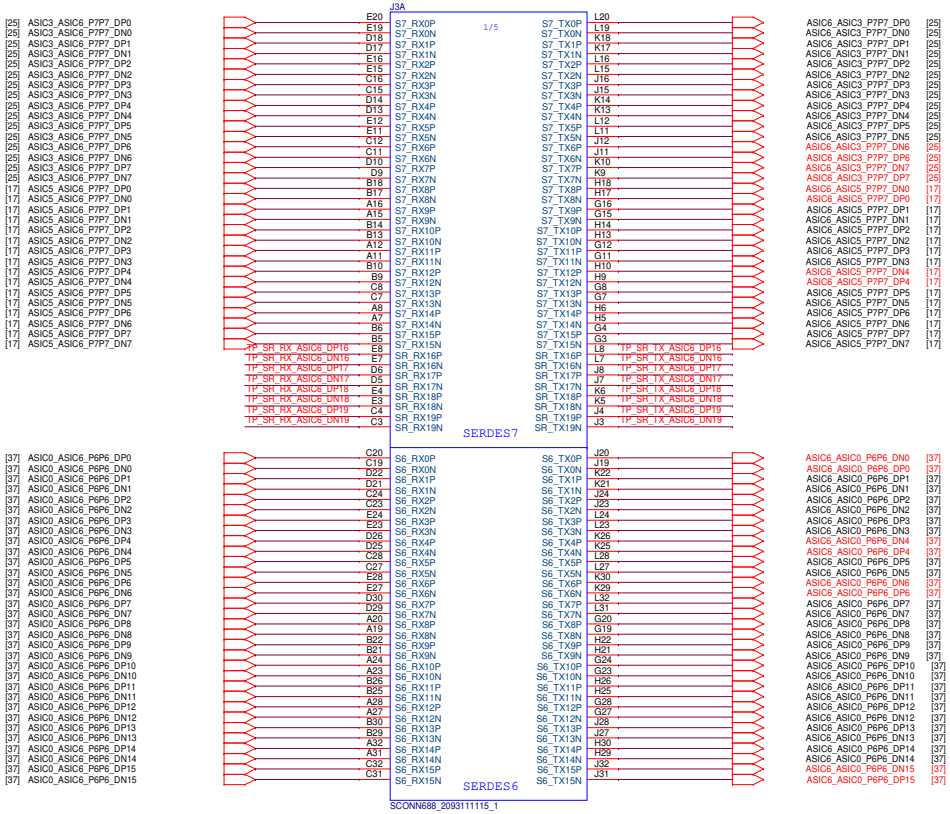
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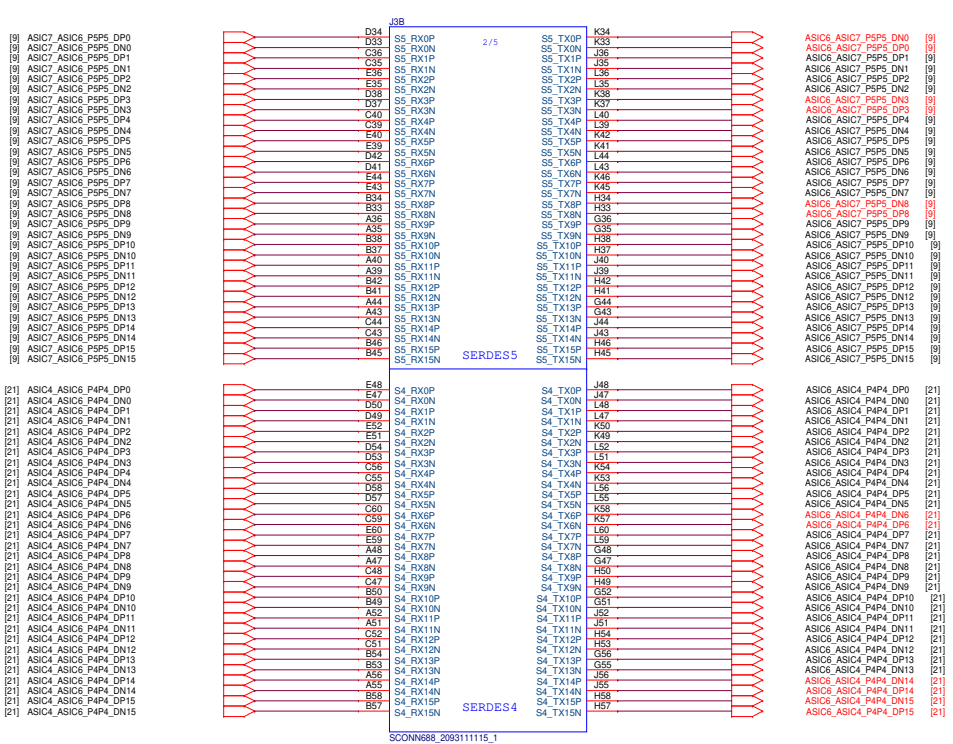
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		Reviewer: <Reviewer>	Size	Date: Tuesday, January 18, 2022
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ASIC7_PWR/GND

Quanta	Department: CCBU	Designer: <Designer>	Project: <project_name>	Doc Number: EP_BASEBOARD_OCP
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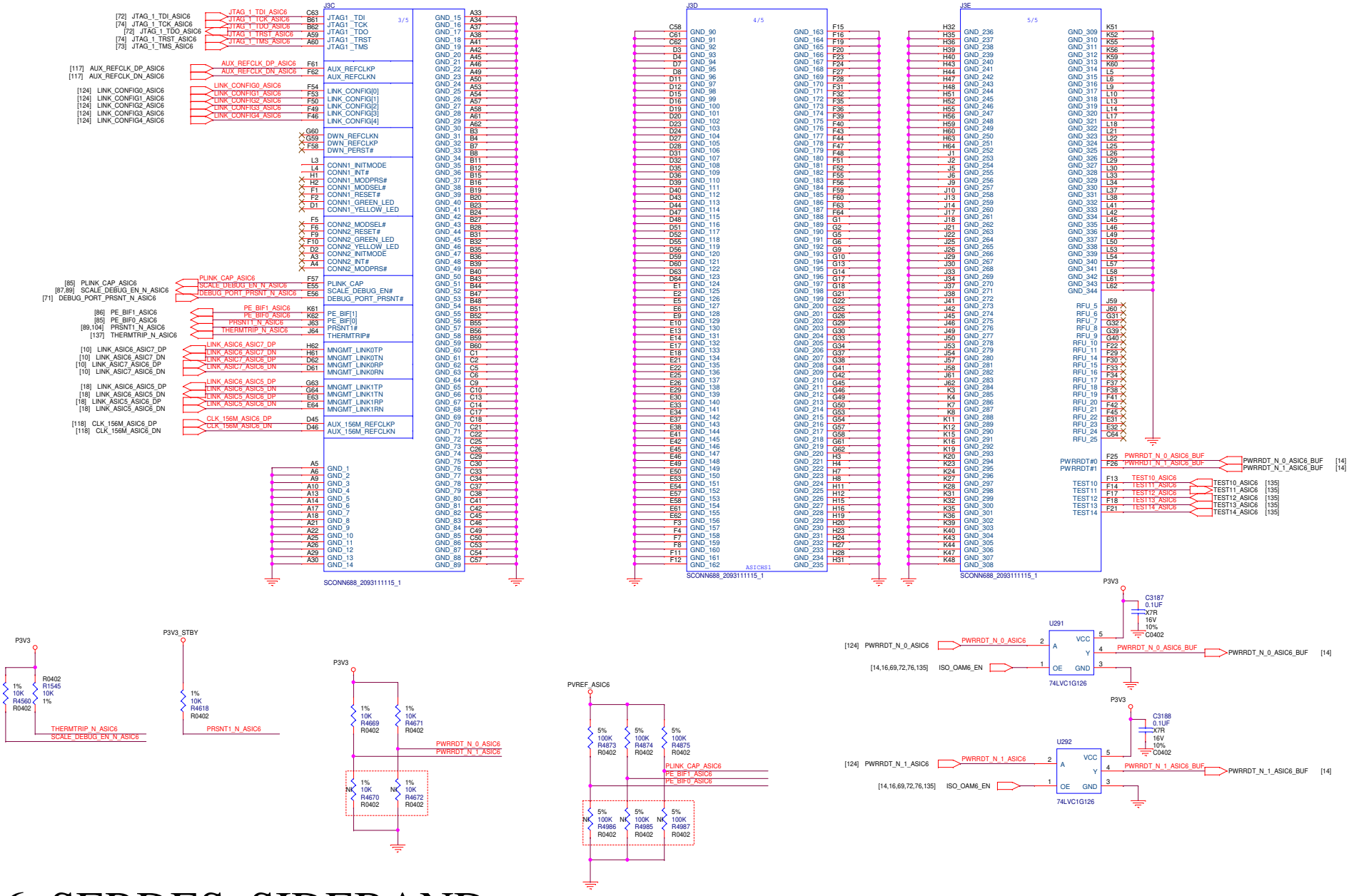




NOTE:Polarity reversal is marked in red

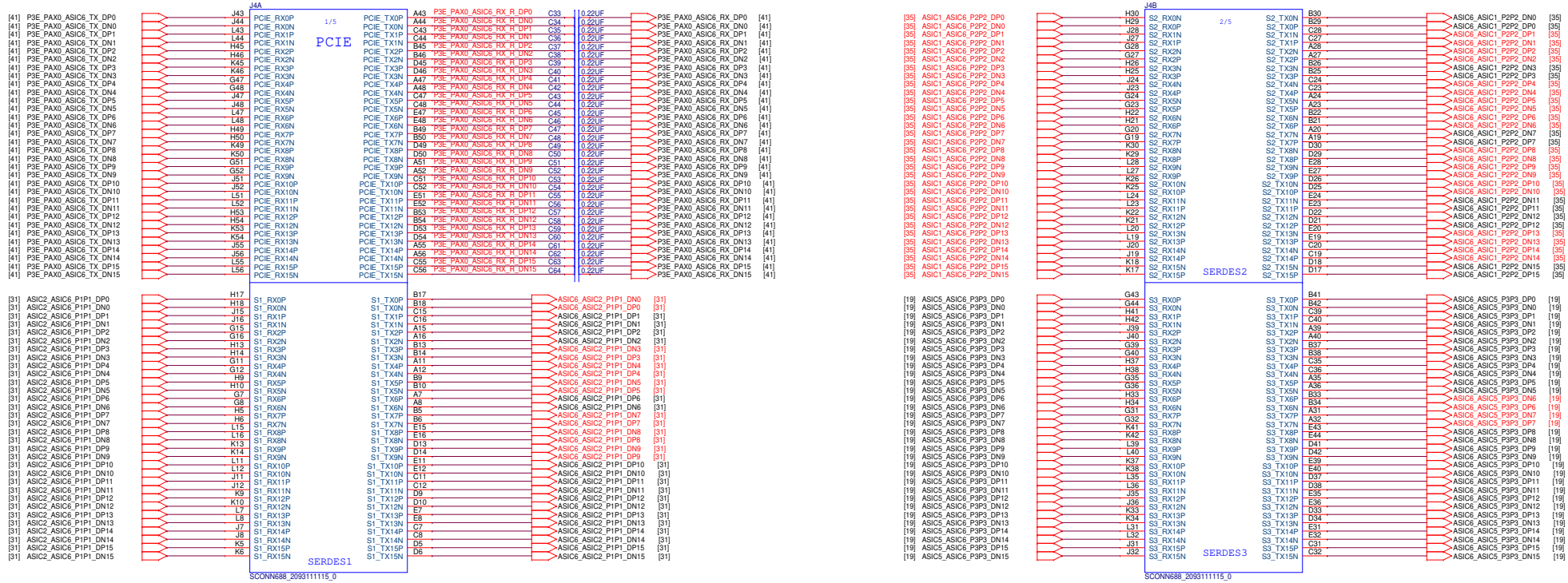
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Quanta	Department: CCBU	Designer: <Designer>	Project: <project_name>	Doc Number: EP_BASEBOARD_OCP
		Reviewer: <Reviewer>	Size	Date: Tuesday, January 18, 2022
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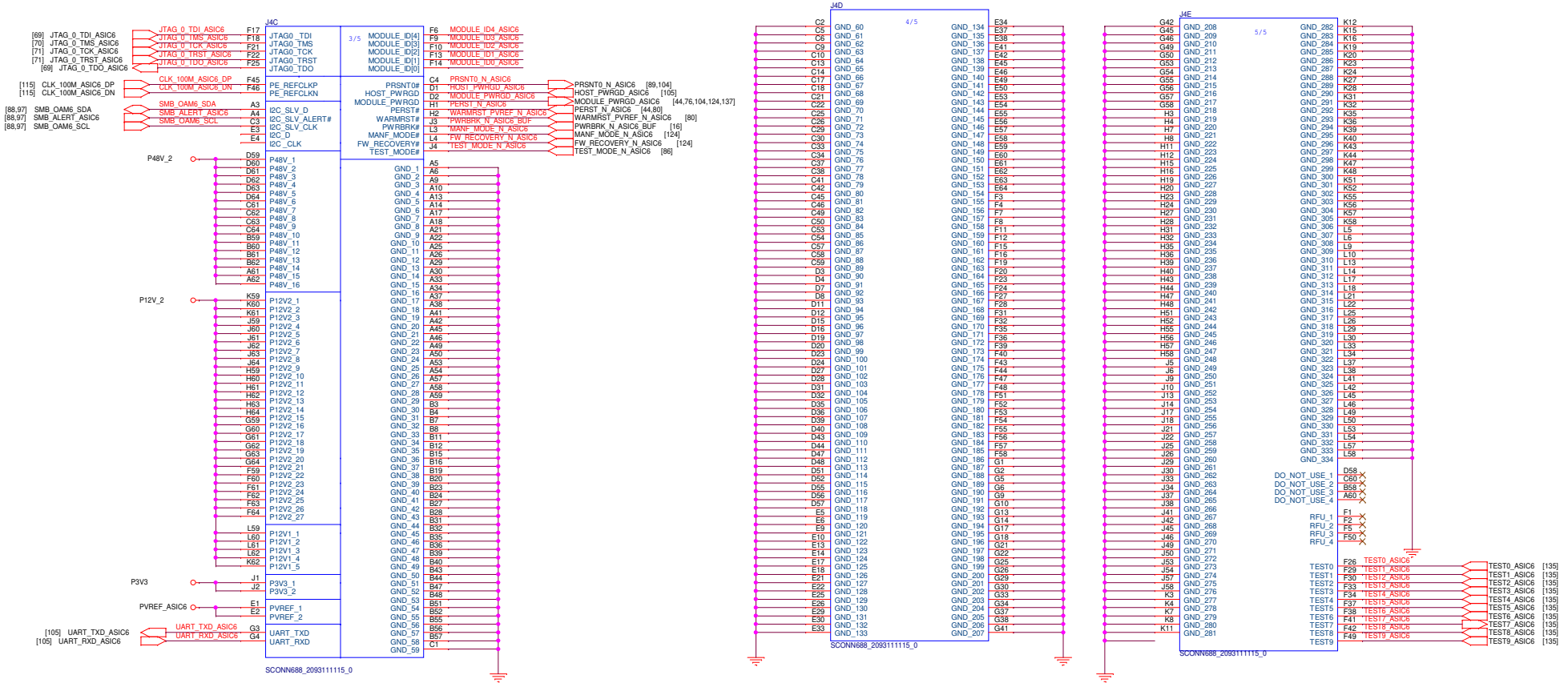
ASIC6_SERDES_SIDEBAND

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ASIC6_PCIE

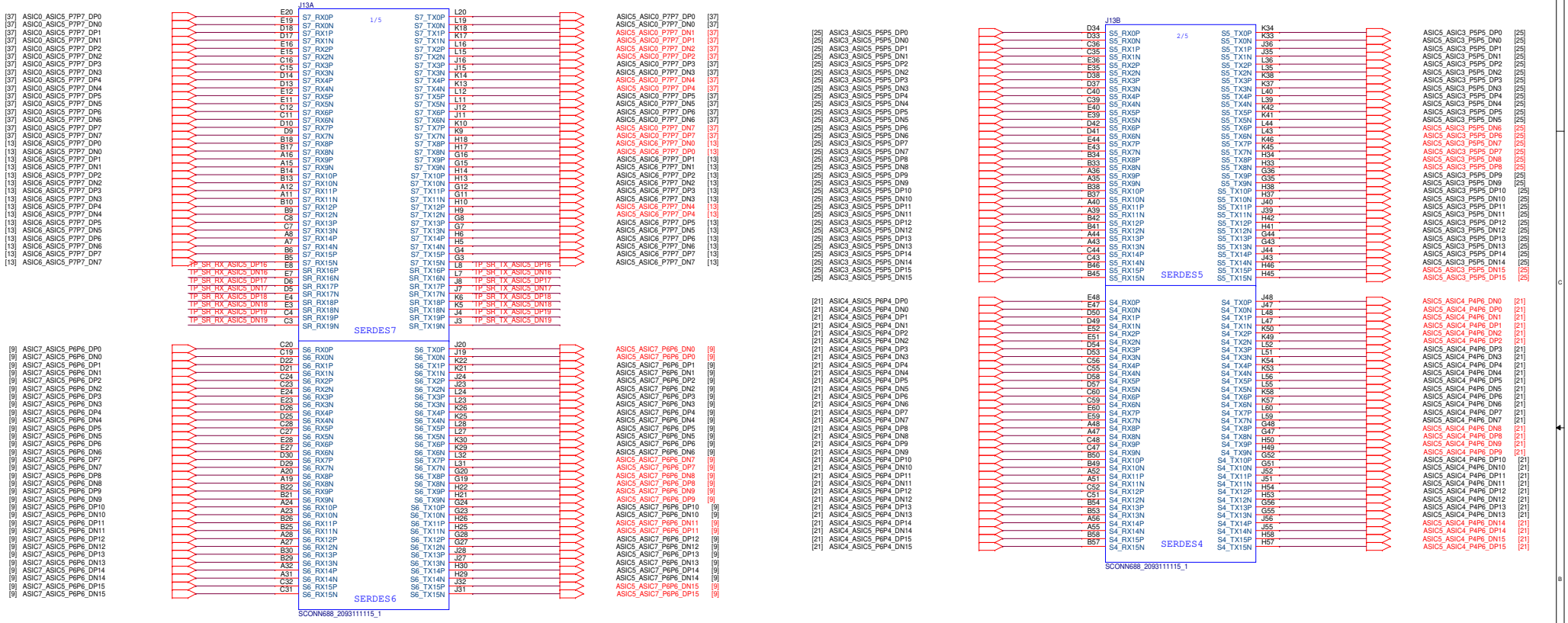
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ASIC6_PWR_GND

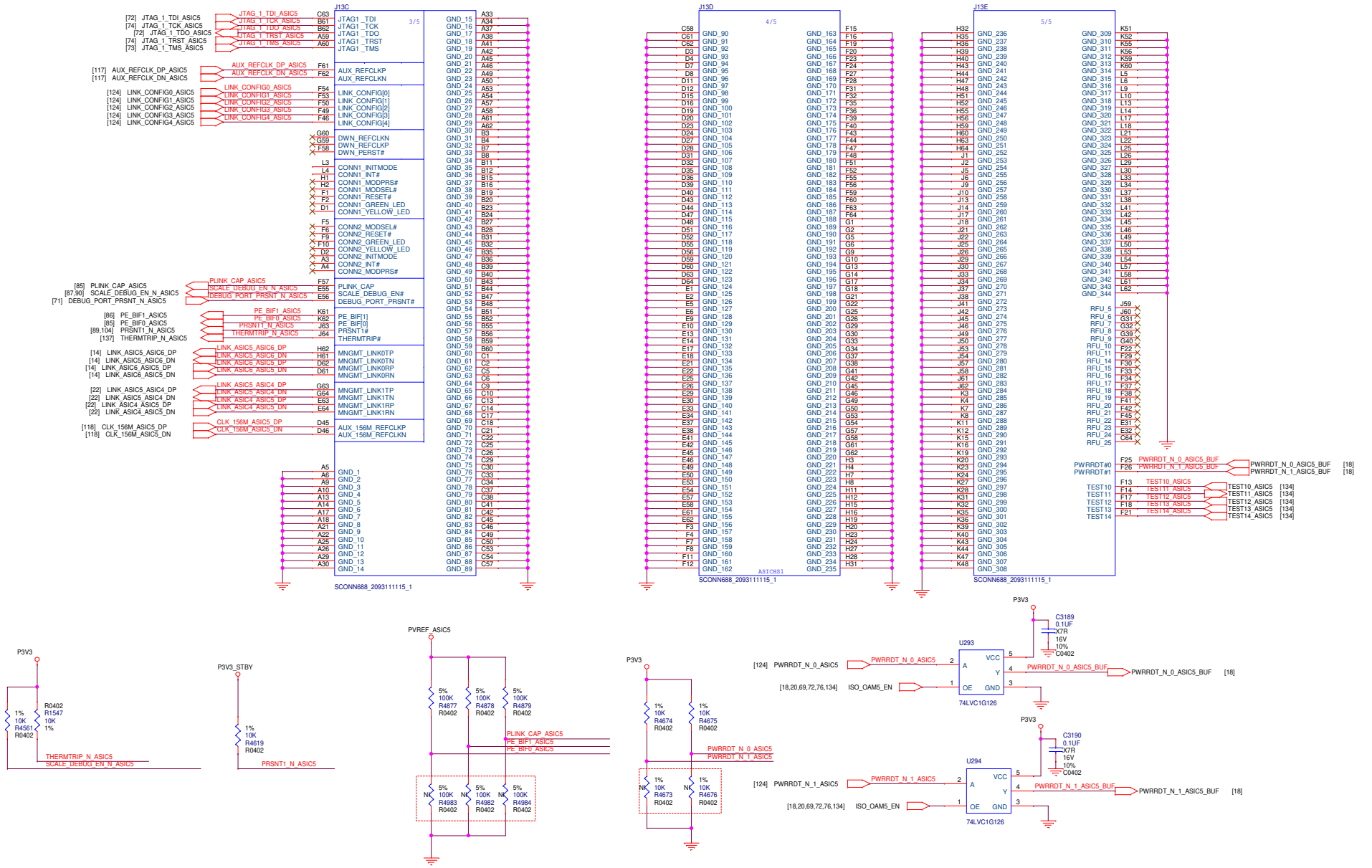
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		Reviewer: <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title: Cover Page — Sheet 16 of 155



NOTE:Polarity reversal is marked in red

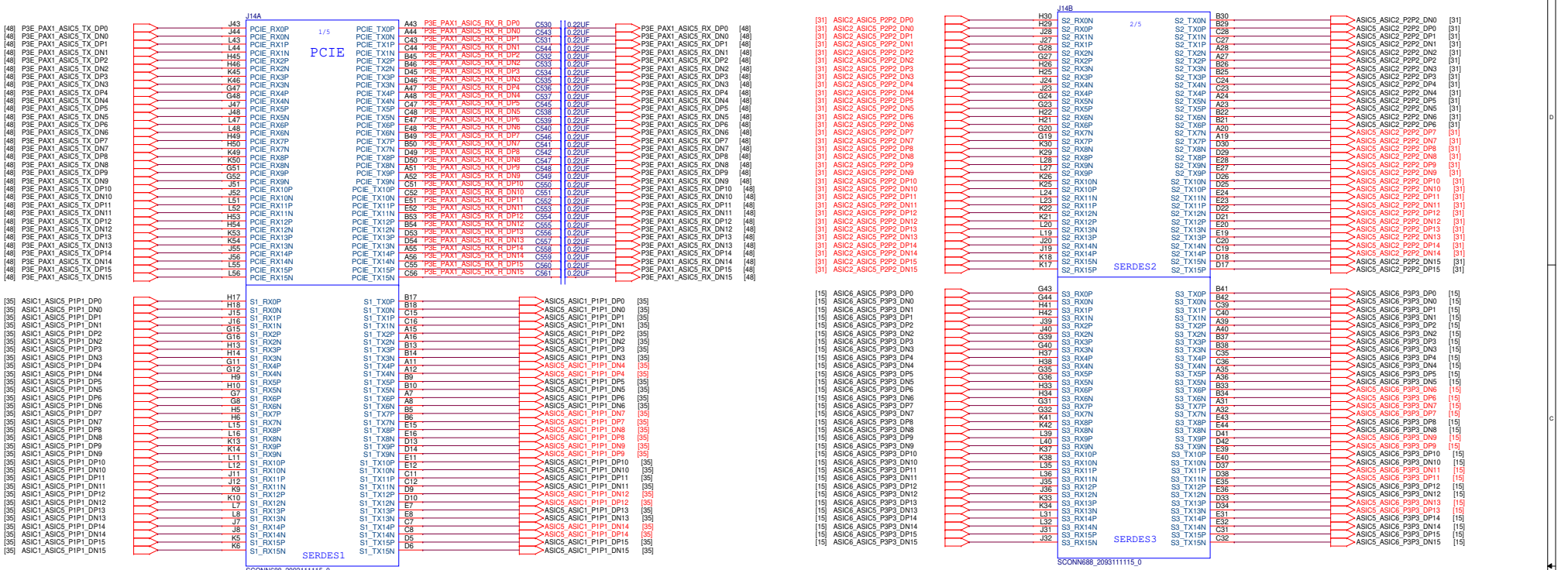
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Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 17 of 155



ASIC5_SERDES_SIDEBAND

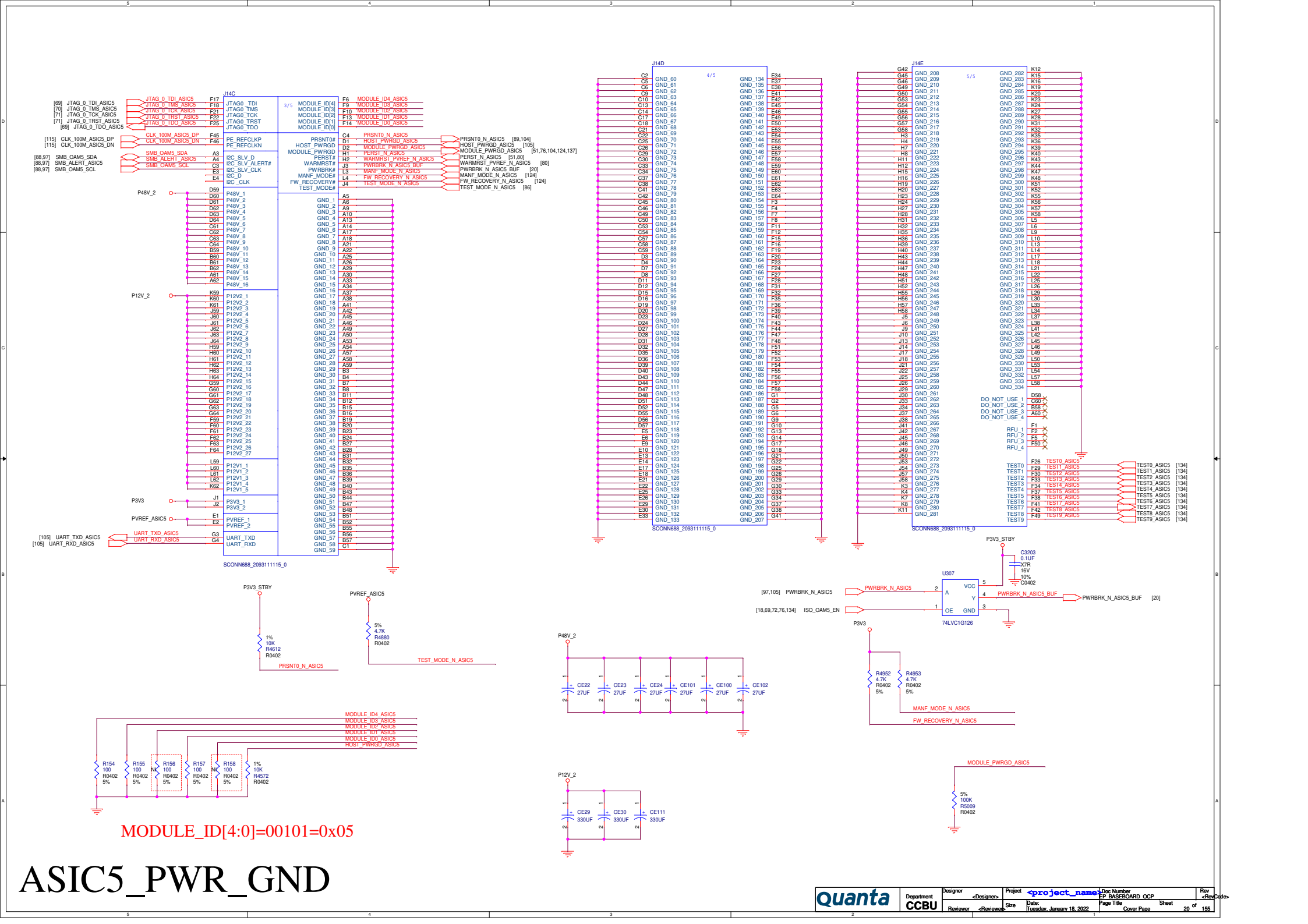
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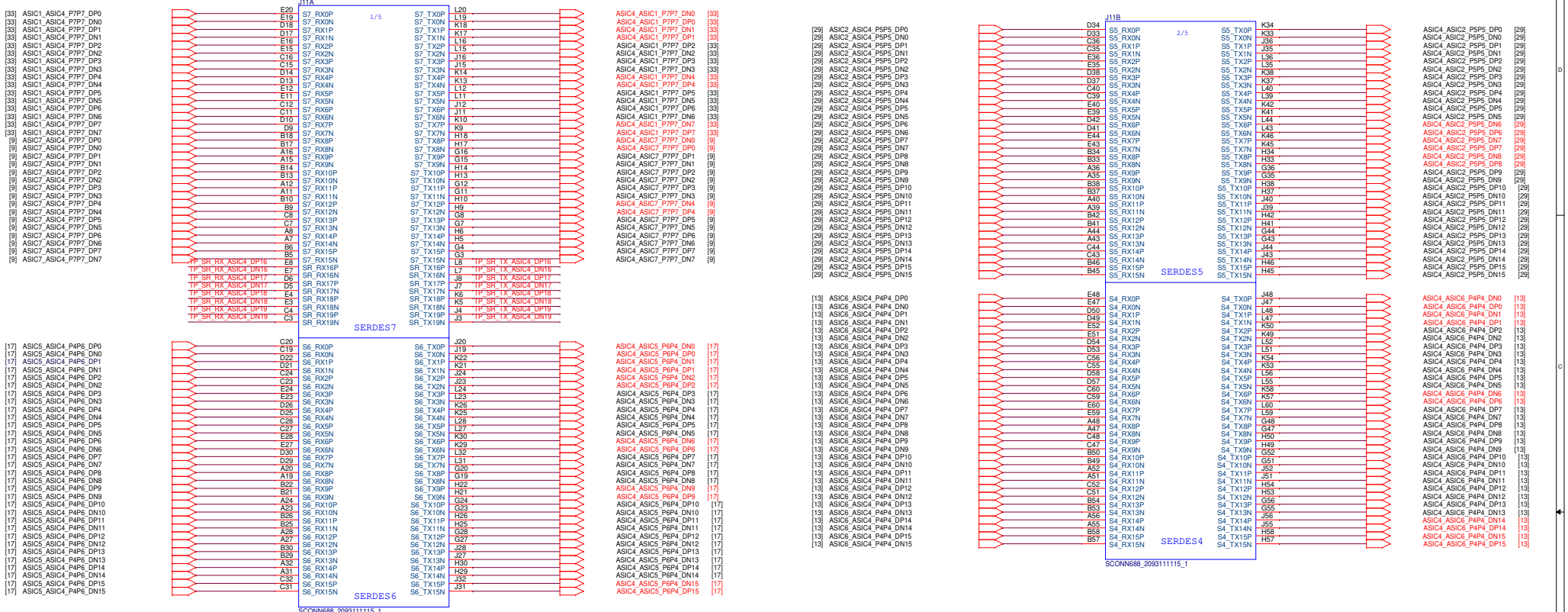
NOTE:Polarity reversal is marked in red

ASIC5_PCIE

Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 19 of 155

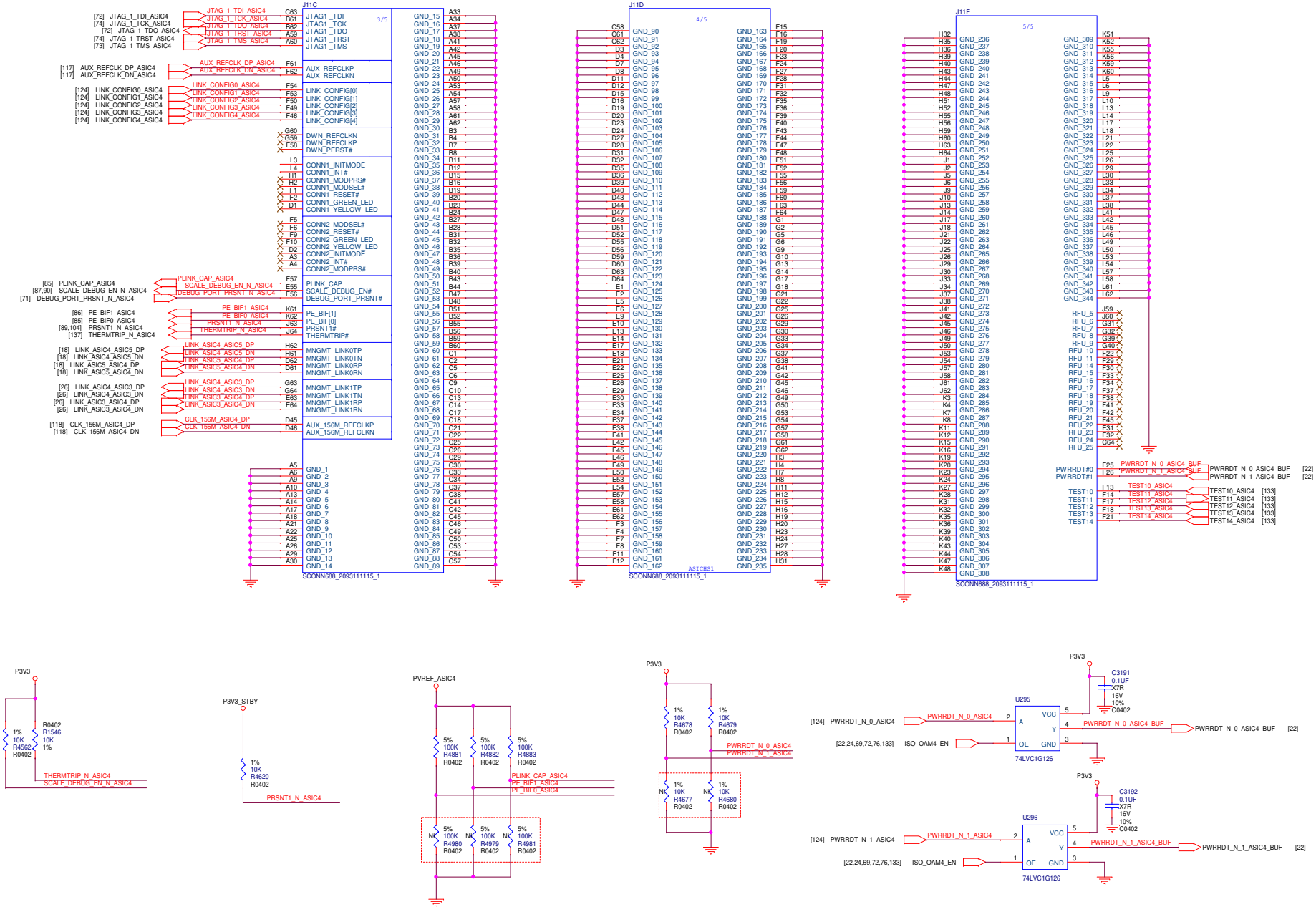


Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP
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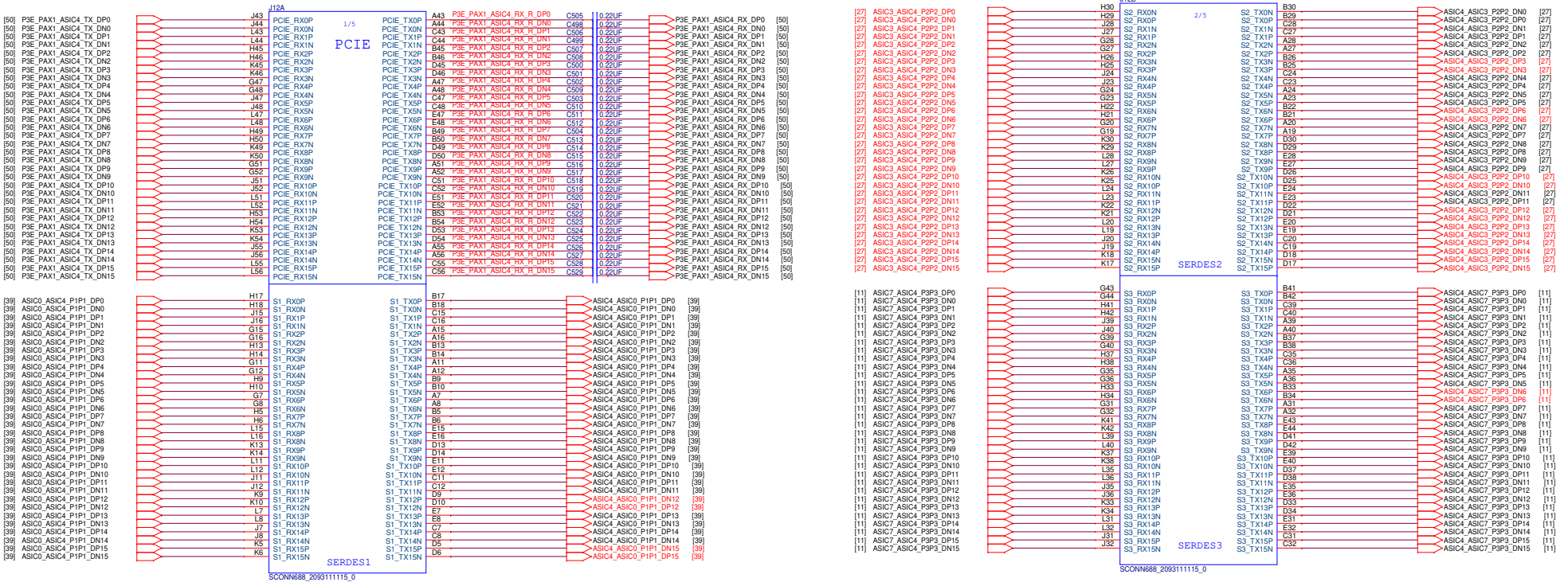
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ASIC4_SERDES_SIDEBAND

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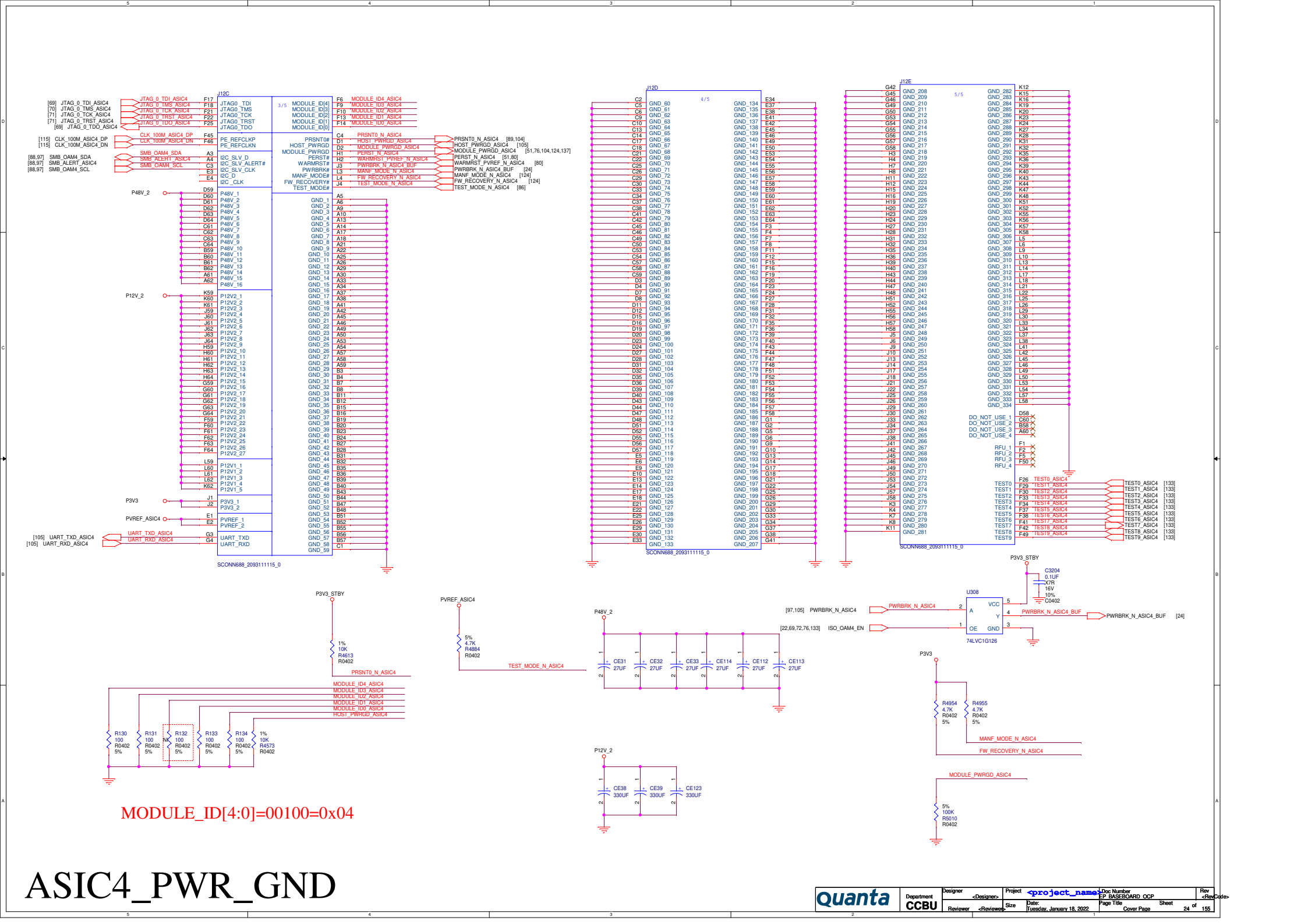


NOTE:Polarity reversal is marked in red

ASIC4_PCIE

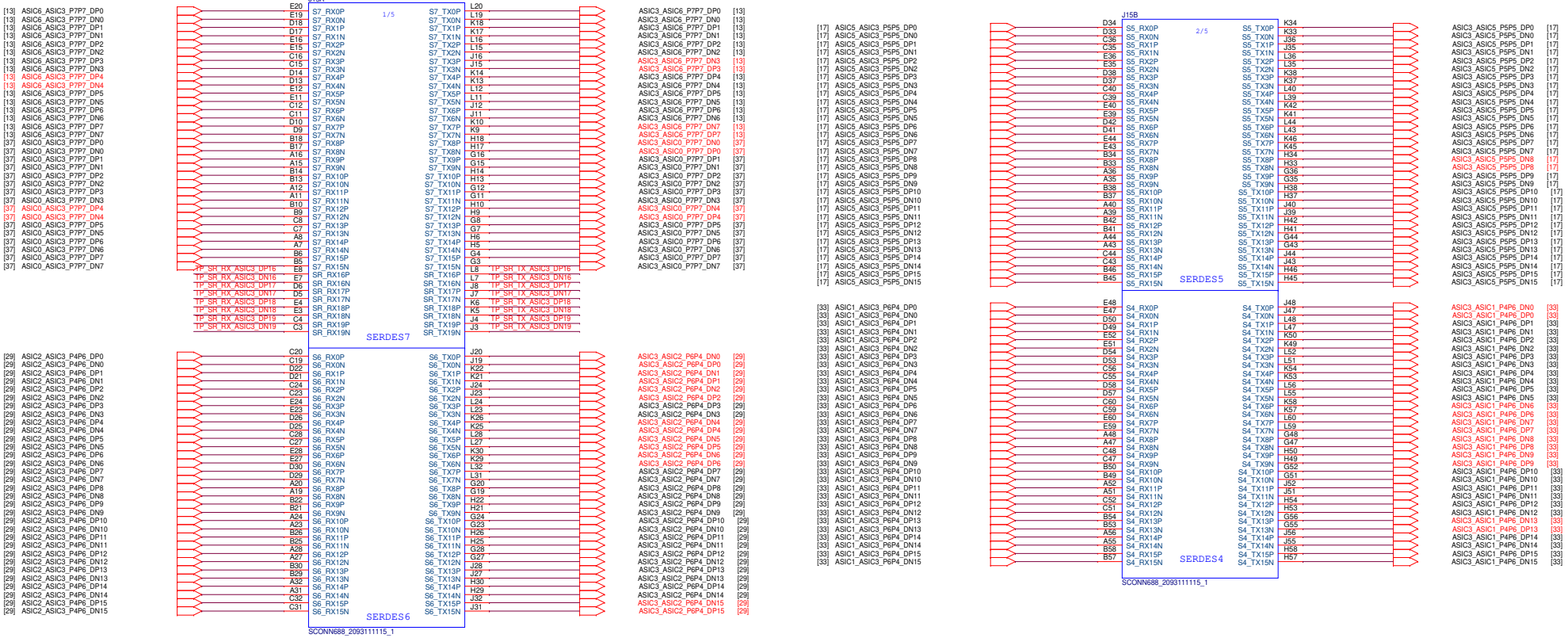
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		Reviewer: <Reviewer>	Size	Date: Tuesday, January 18, 2022
				Page Title: Cover Page

Rev: <RevCode>
Sheet 23 of 155



ASIC4_PWR_GND

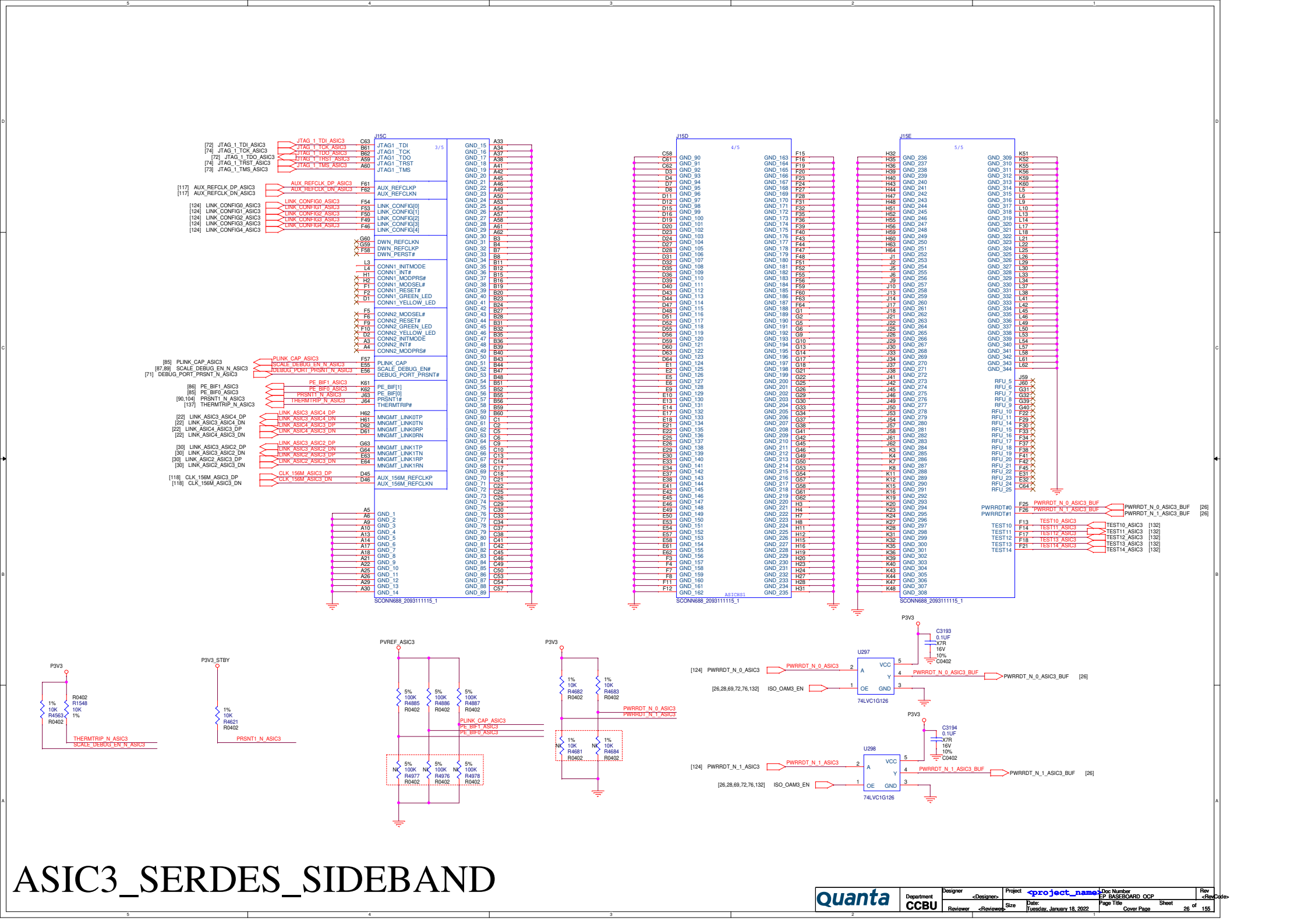
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		Reviewer: <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title: Cover Page Sheet 24 of 155



NOTE:Polarity reversal is marked in red

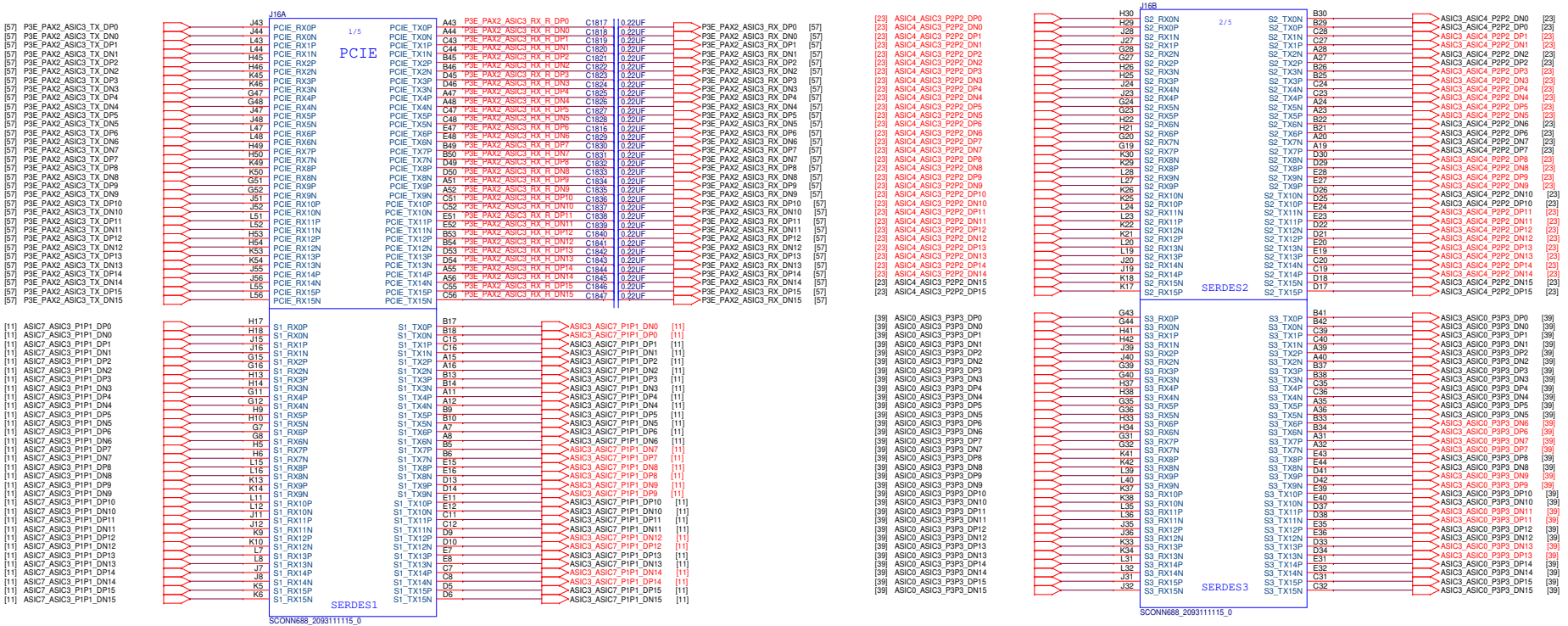
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Quanta	Department: CCBU	Designer: <Designer>	Project: <project_name>	Doc Number: EP_BASEBOARD_OCP	Rev: <RevCode>
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ASIC3_SERDES_SIDEBAND

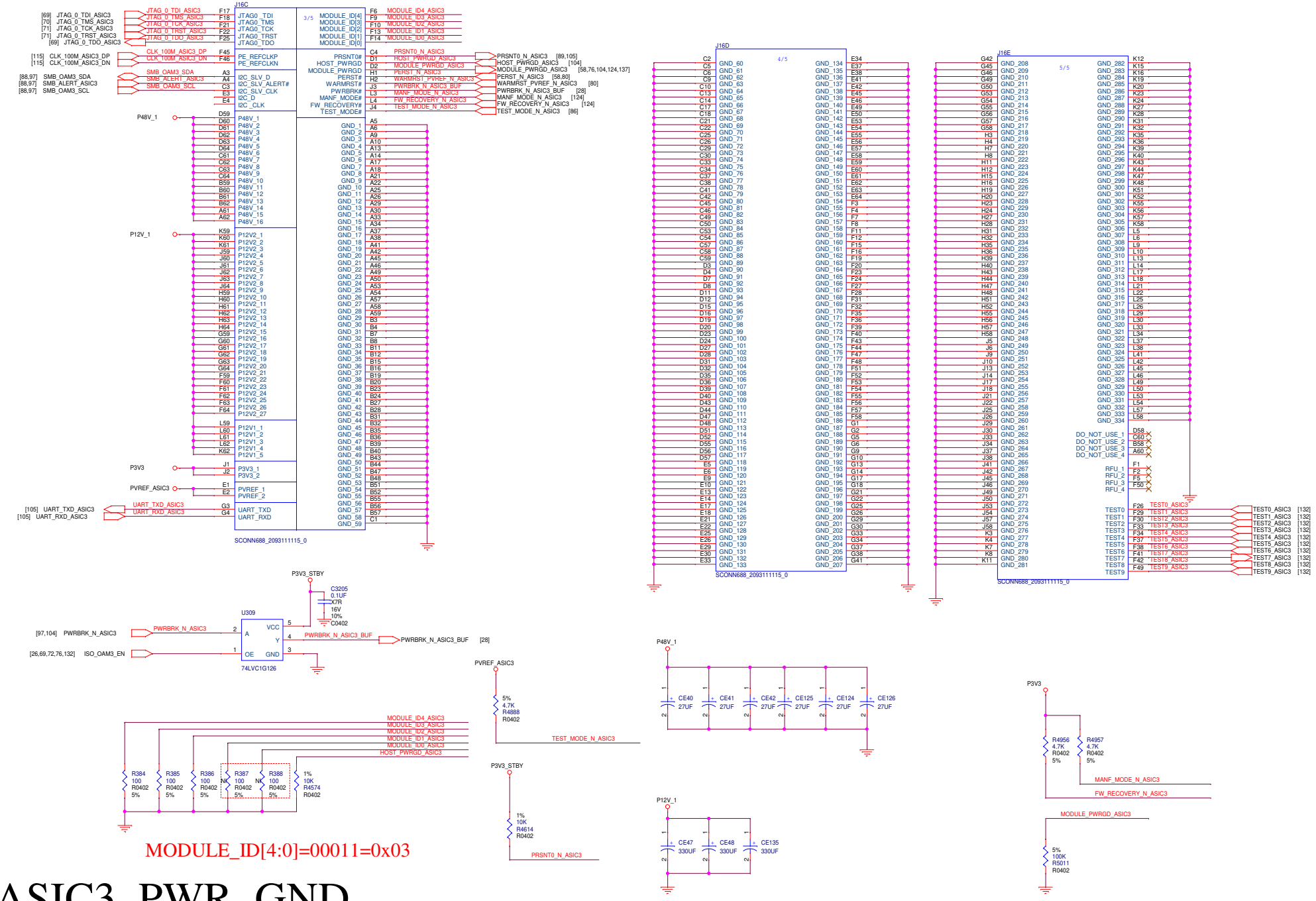
Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 26 of 155



NOTE:Polarity reversal is marked in red

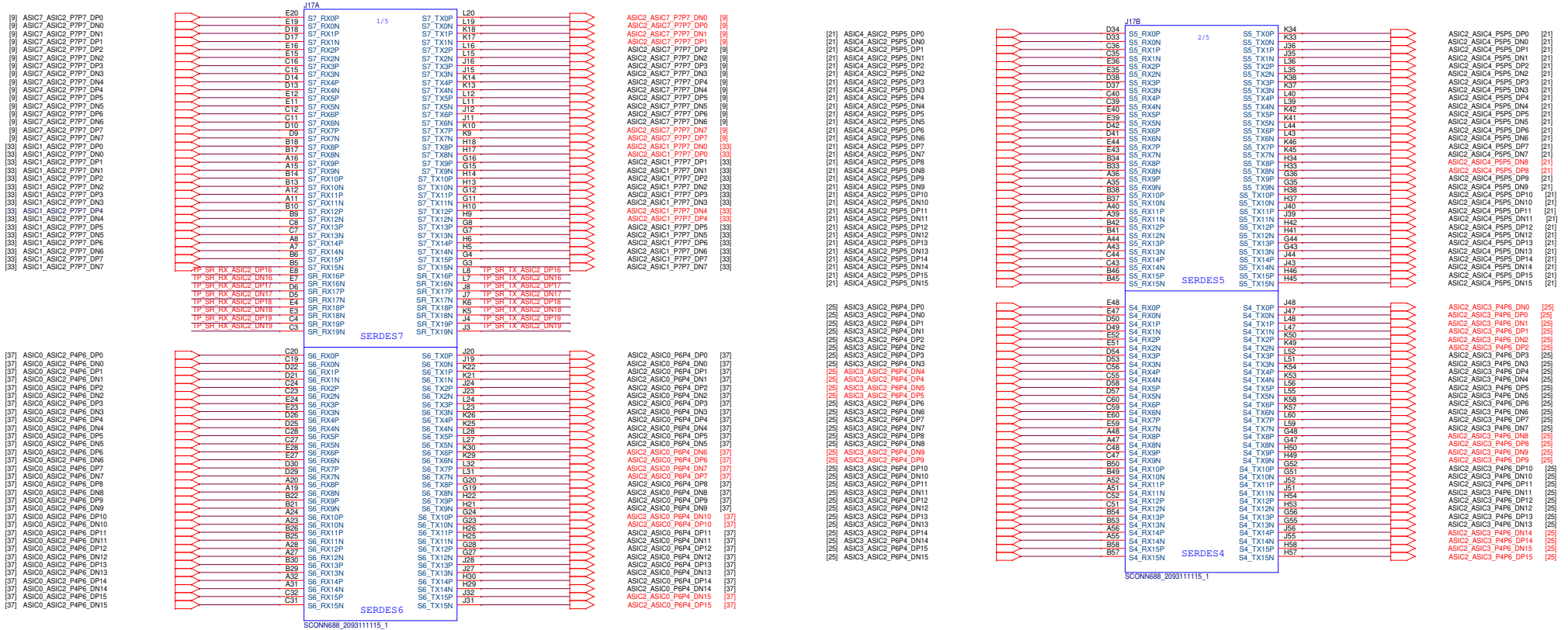
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Quanta	Department: CCBU	Designer: <Designer>	Project: <project_name>	Doc Number: EP_BASEBOARD_OCP
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ASIC3_PWR_GND

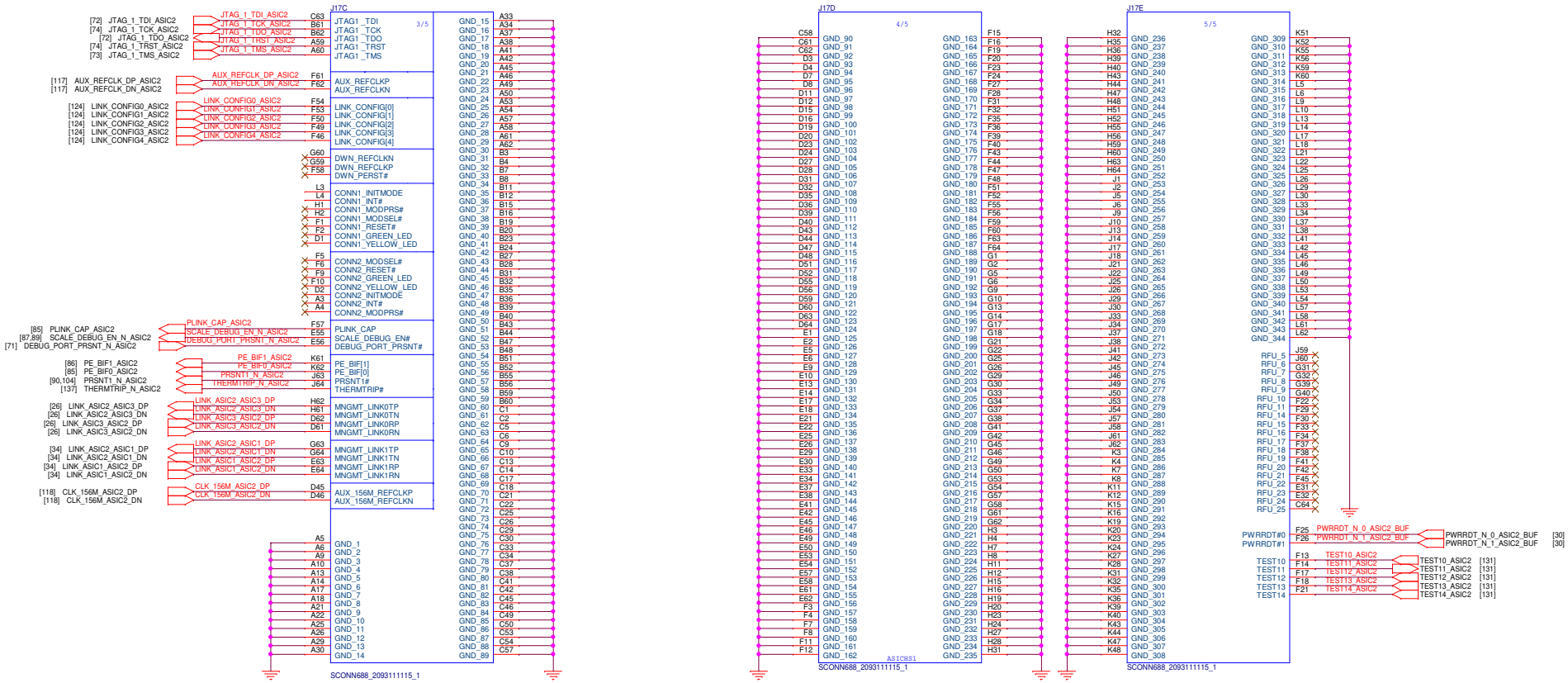
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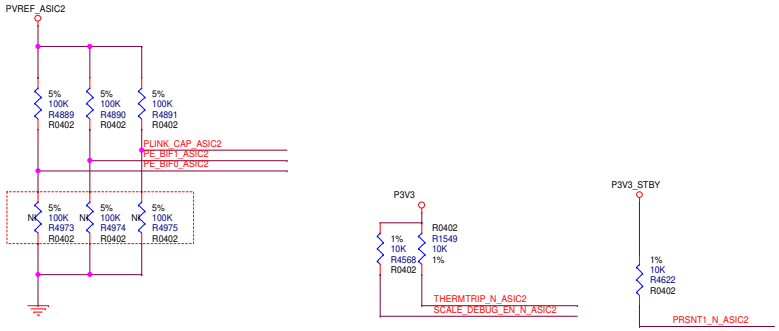


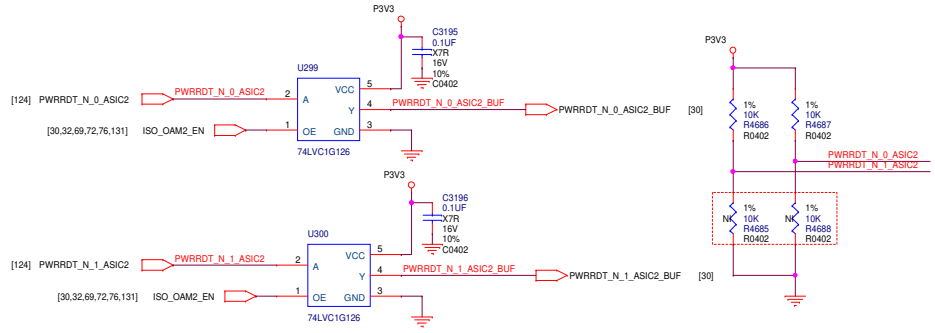
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ASIC2_SERDES

Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
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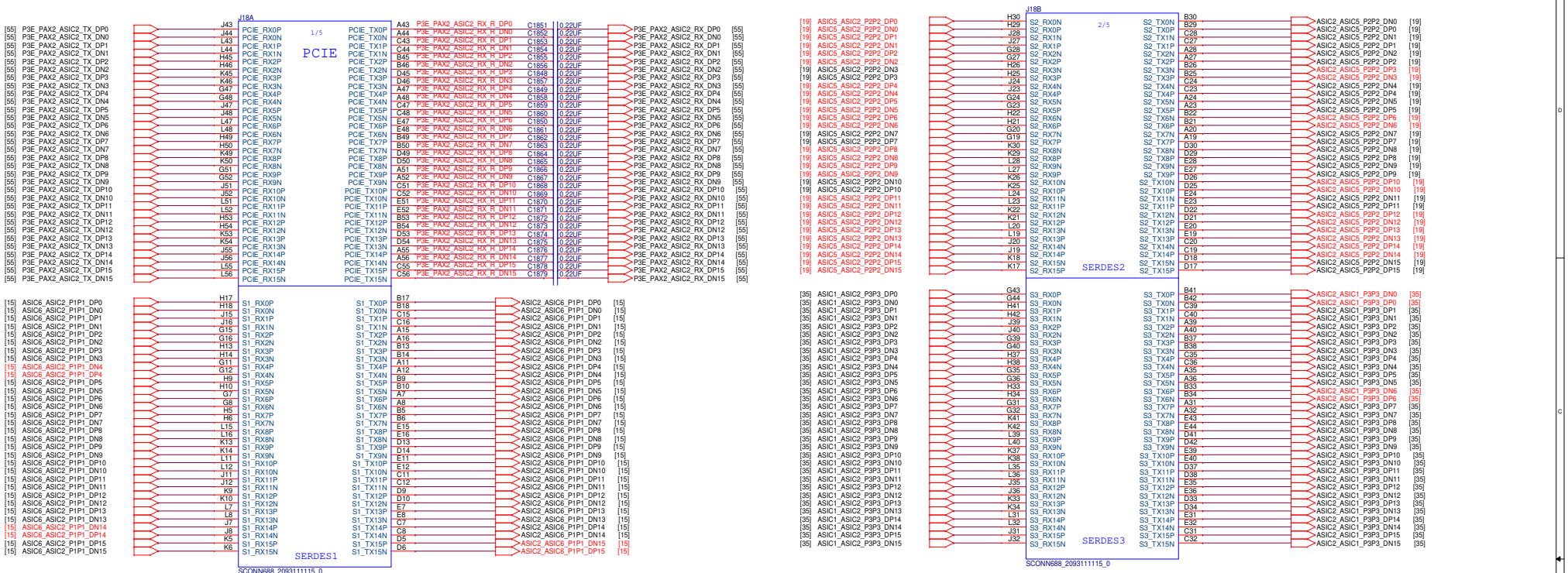






ASIC2_SERDES_SIDEBAND

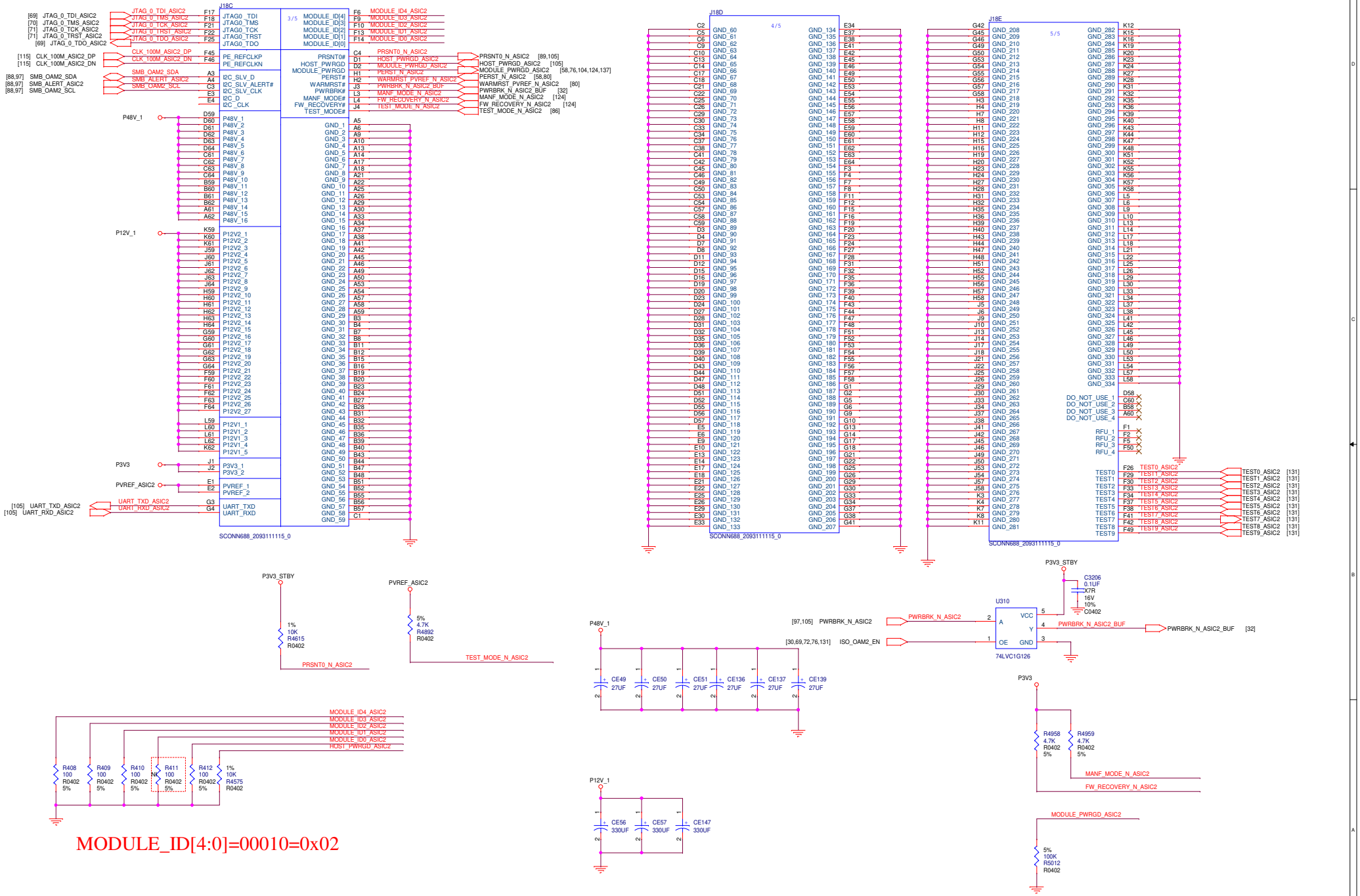
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NOTE:Polarity reversal is marked in red

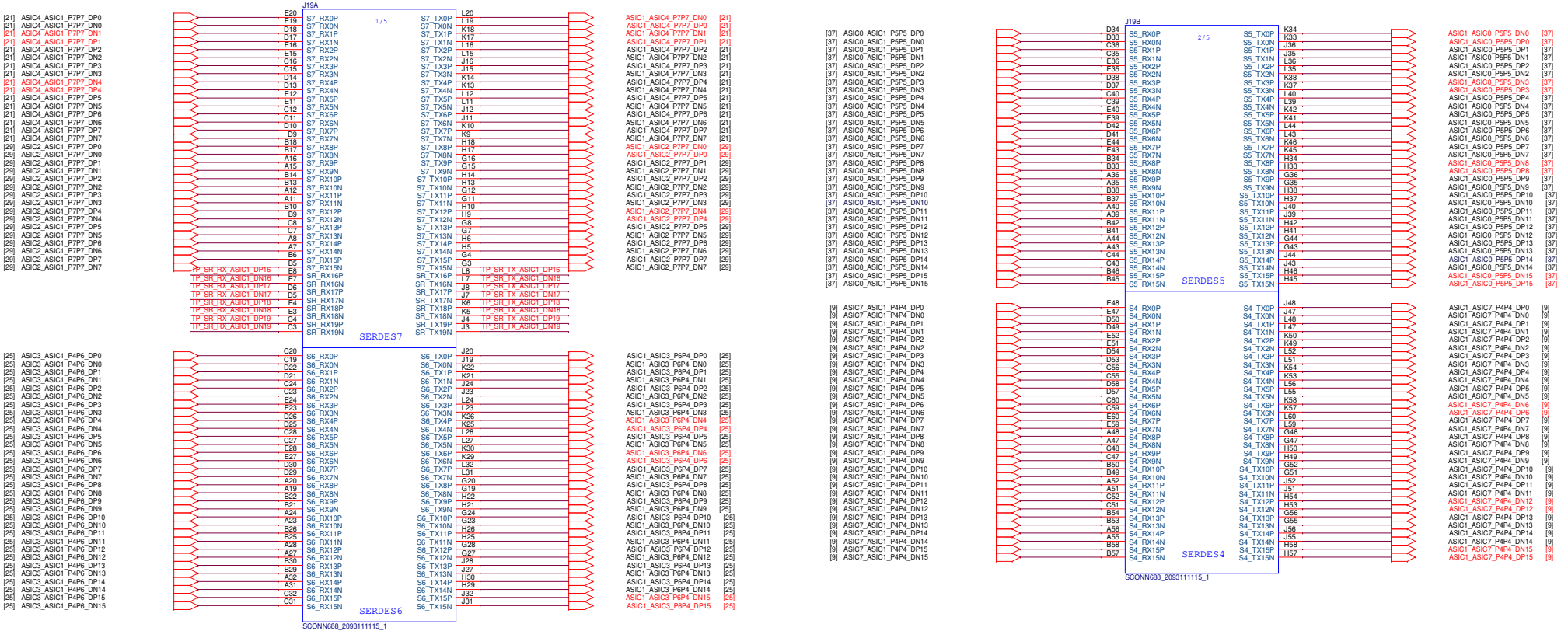
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Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
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ASIC2_PWR_GND

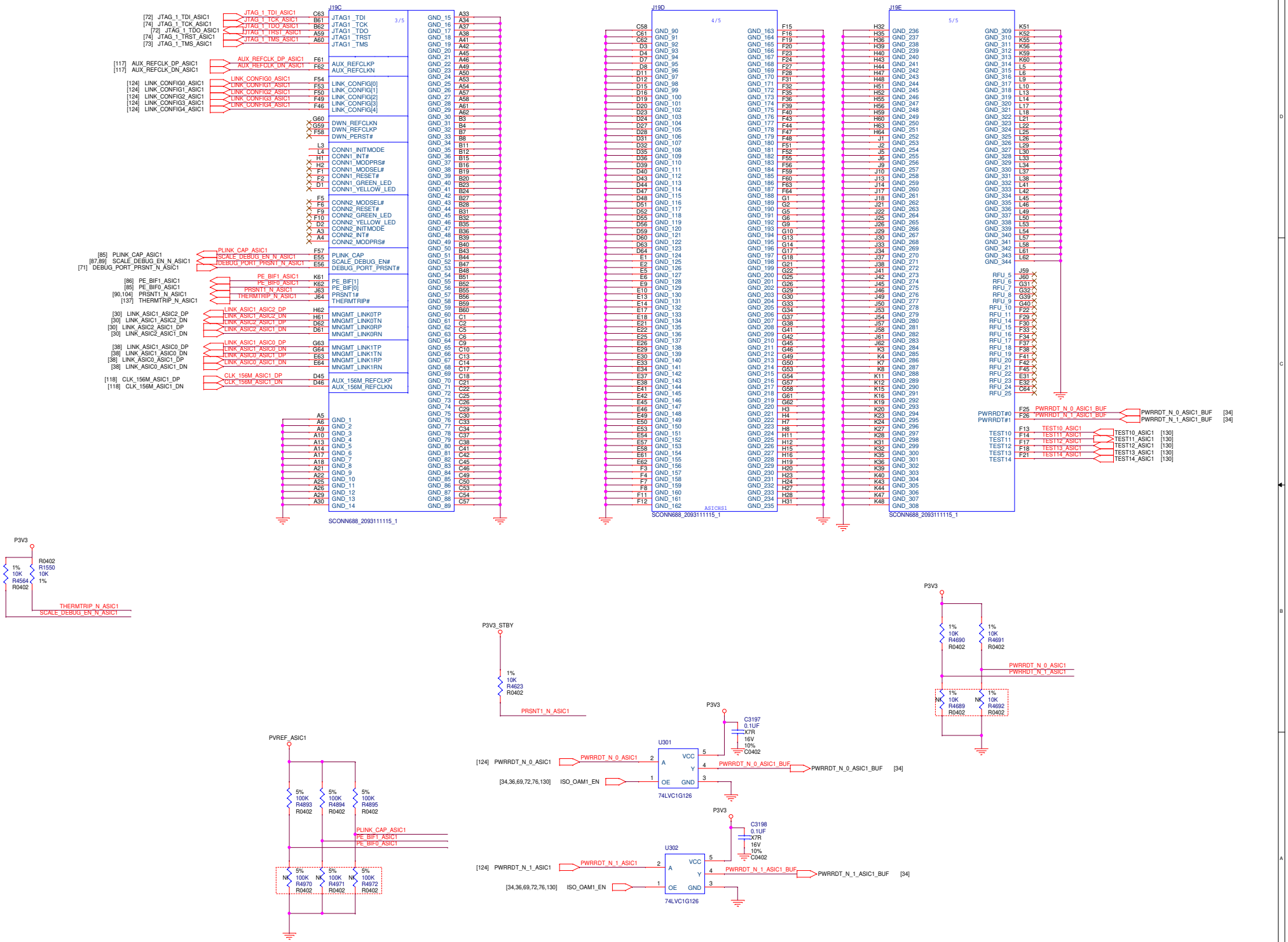
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		Reviewer <Reviewer>	Size / Date: Tuesday, January 18, 2022	Page Title Cover Page / Sheet 32 of 155



NOTE:Polarity reversal is marked in red

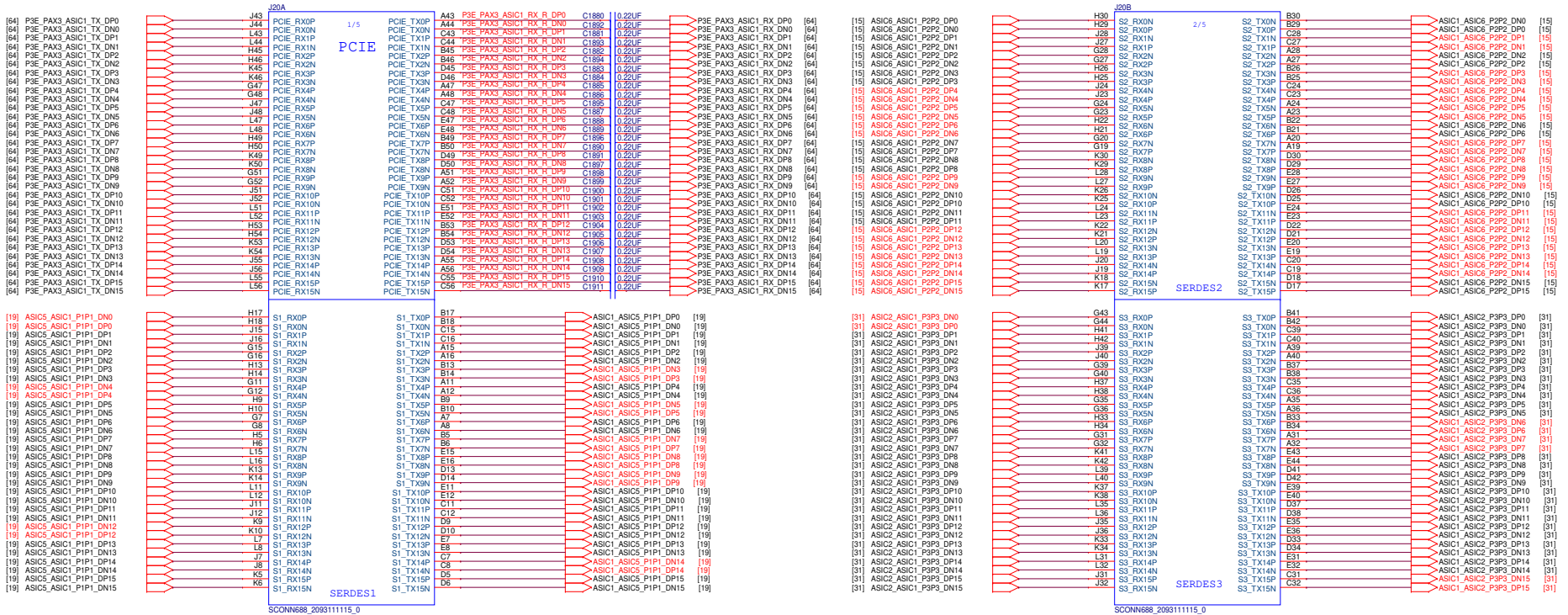
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Quanta	Department: CCBU	Designer: <Designer>	Project: <project_name>	Doc Number: EP_BASEBOARD_OCP	Rev: <RevCode>
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ASIC1_SERDES_SIDEBAND

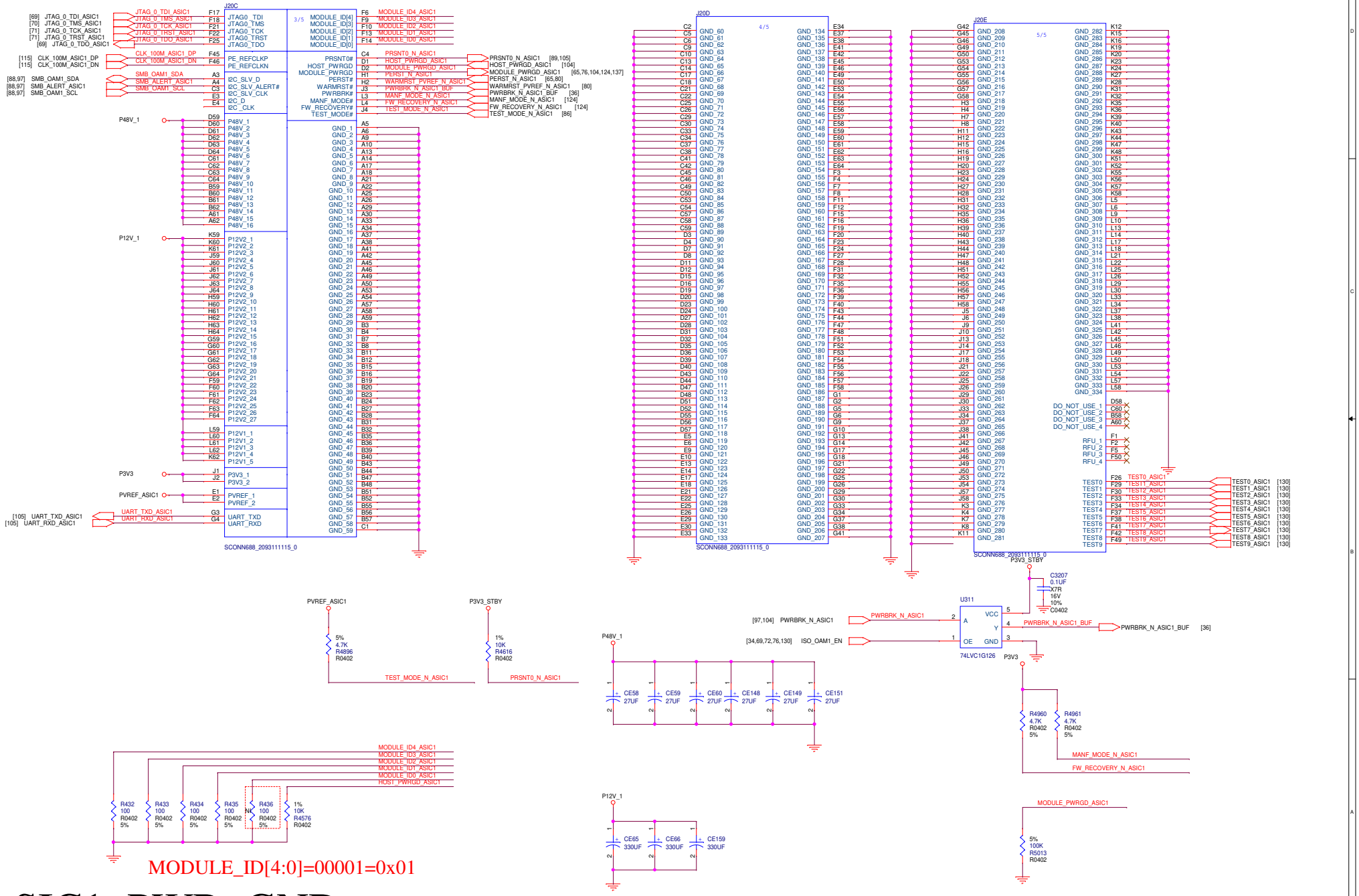
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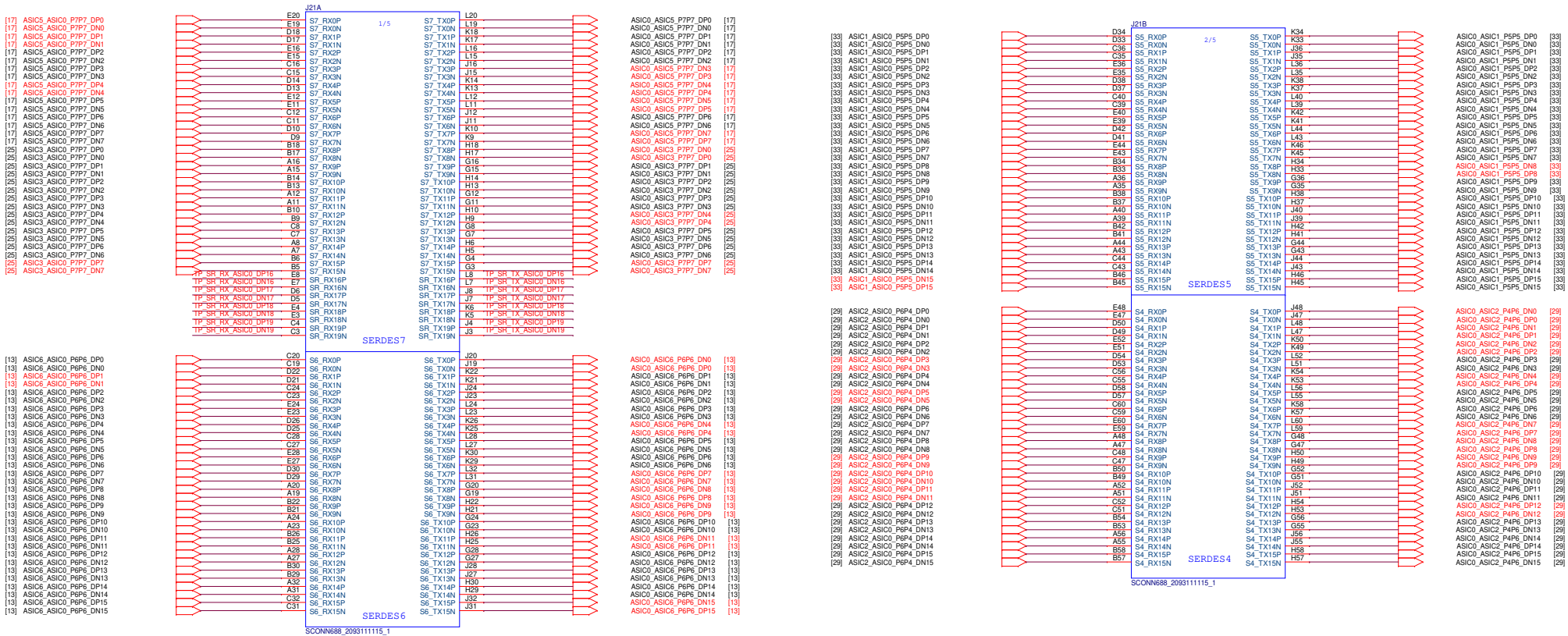
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ASIC1_PCIE

Quanta	Department: CCBU	Designer: <Designer>	Project: <project_name>	Doc Number: EP_BASEBOARD_OCP
		Reviewer: <Reviewer>	Size	Date: Tuesday, January 18, 2022
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				Rev: <RevCode>
				Sheet 35 of 155



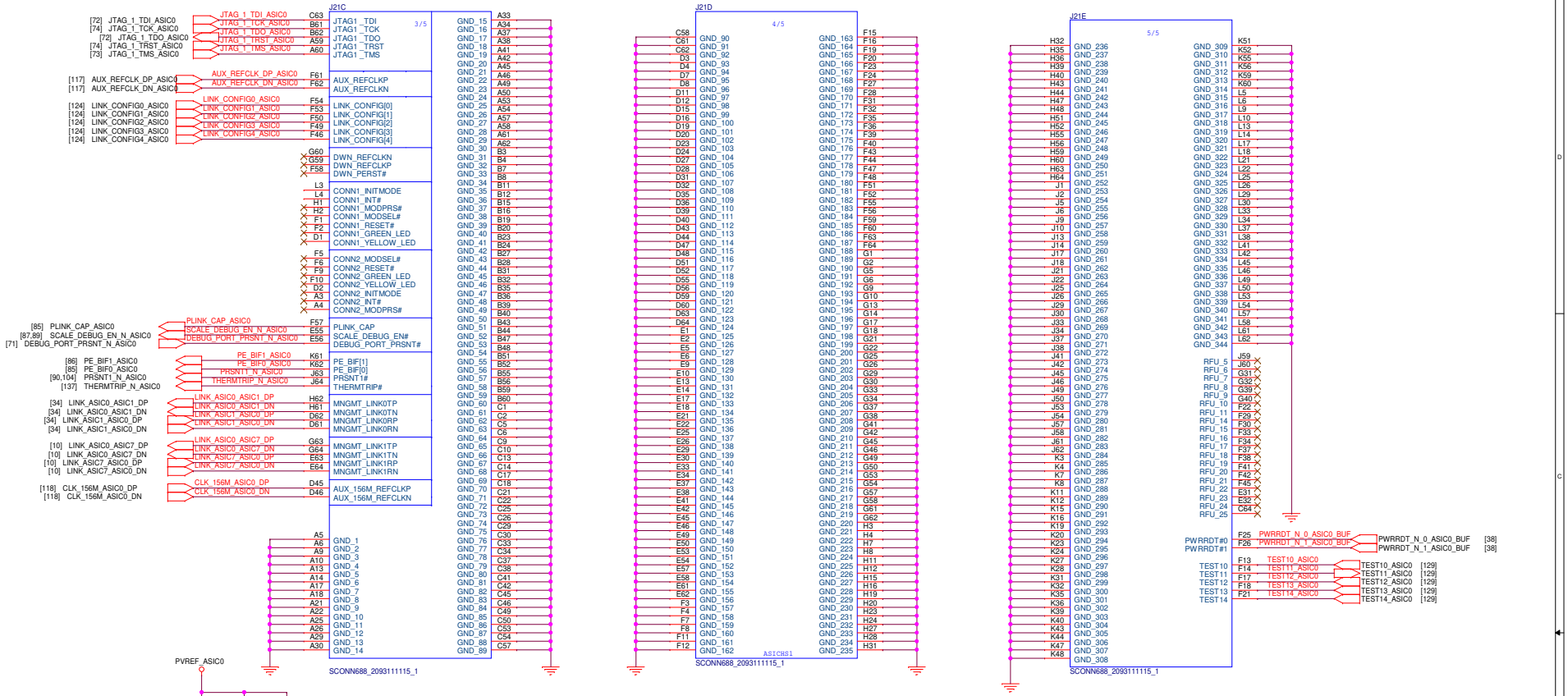
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NOTE:Polarity reversal is marked in red

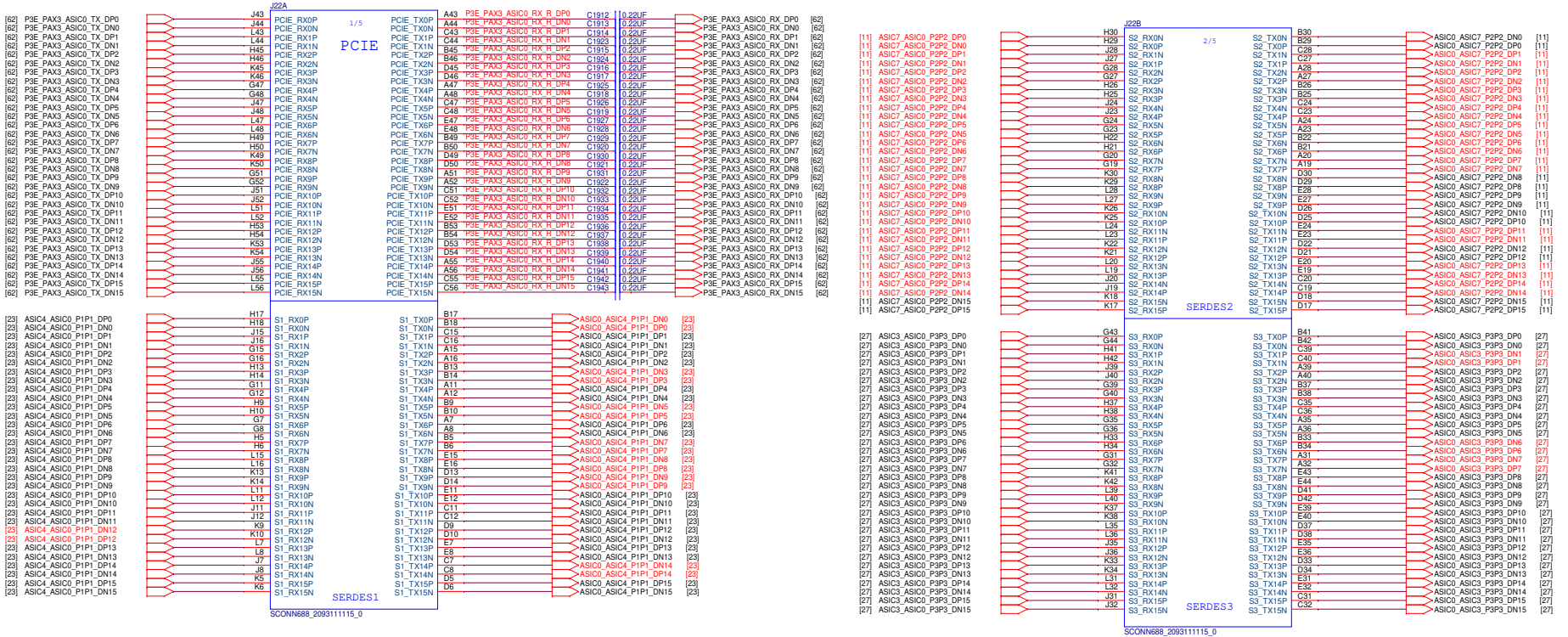
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Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 37 of 155



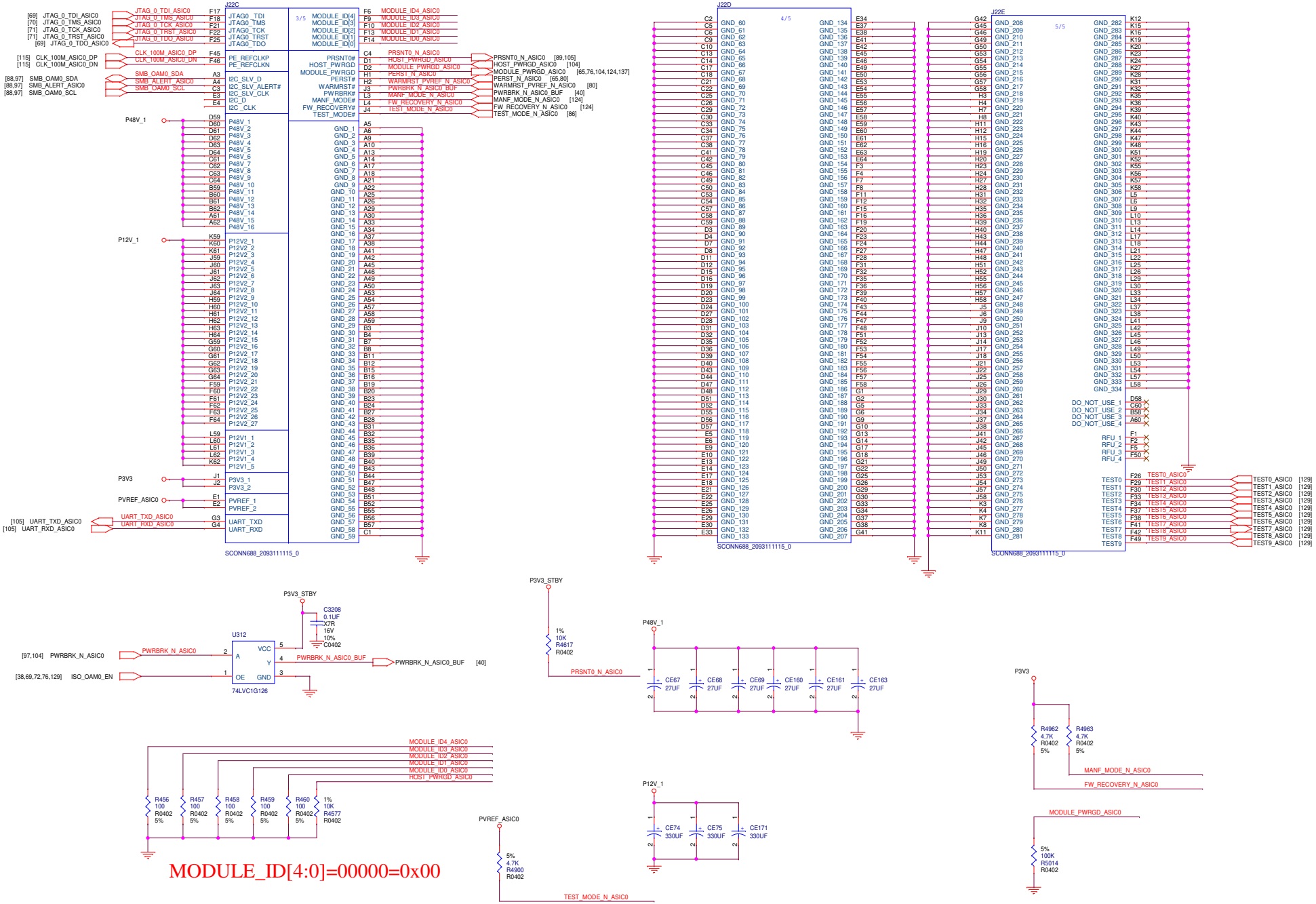
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Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
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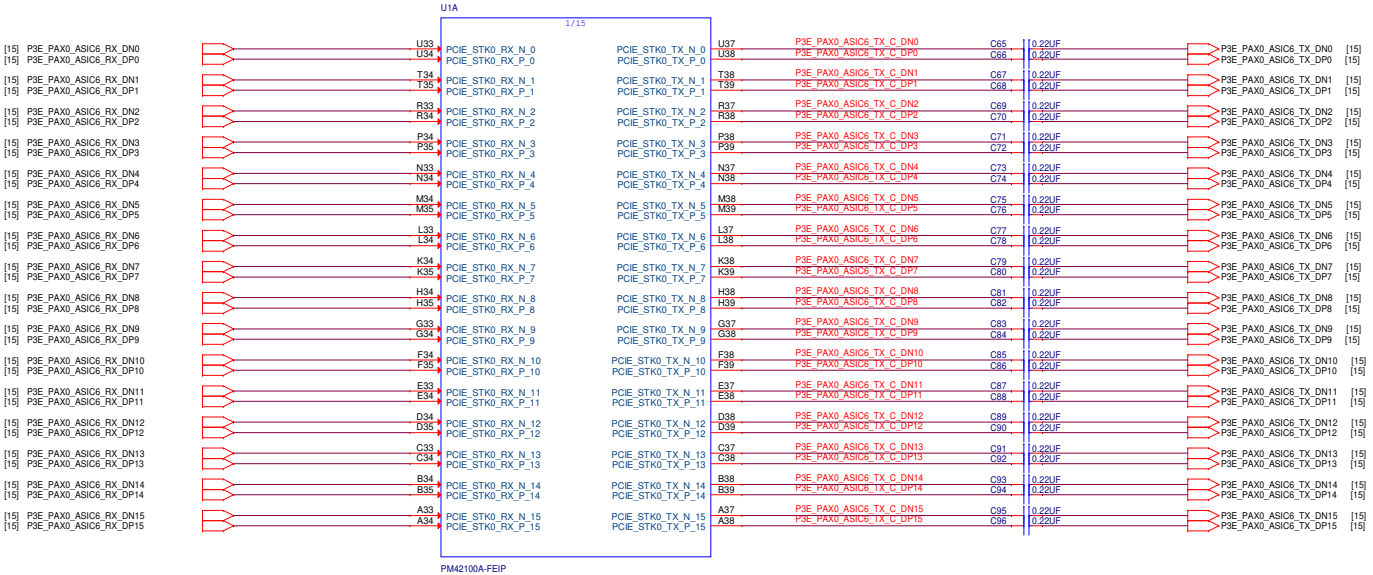
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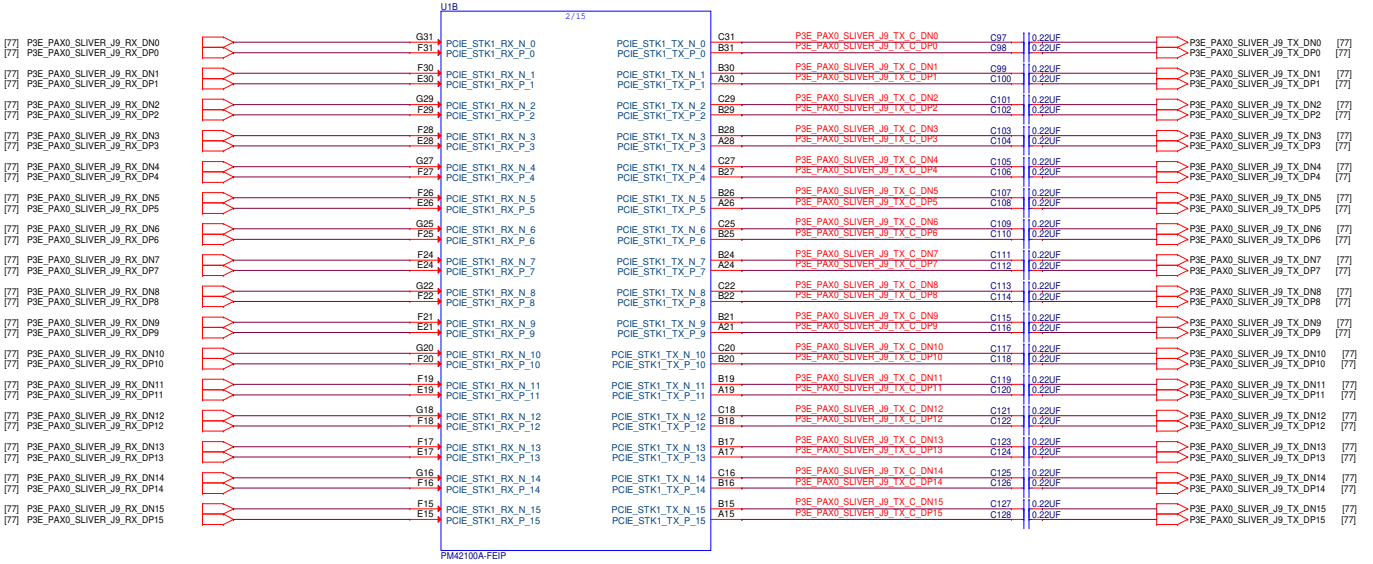


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Quanta	Department: CCBU	Designer: <Designer>	Project: <project_name>	Doc Number: EP_BASEBOARD_OCP	Rev: <RevCode>
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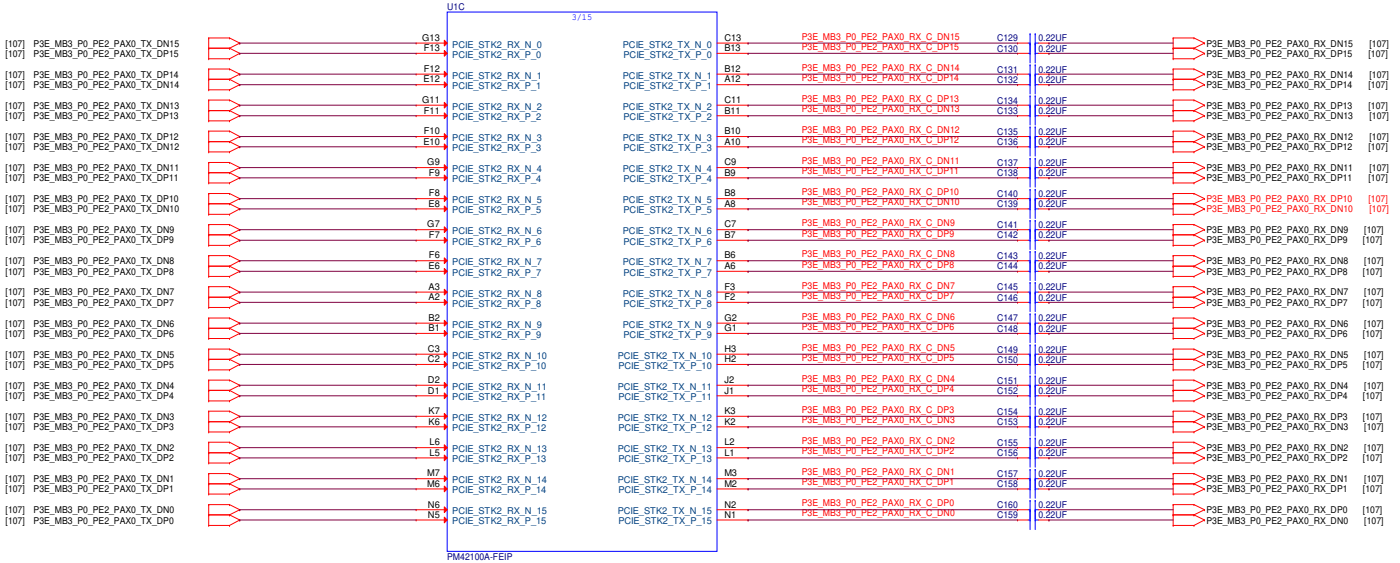
PAX0 TO ASIC6



PAX0 TO SLIVER CONN

PAX0_STATION_0_1

Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 41 of 155



PAX0 TO "MB3 "CPU0



PAX 0 TO MB2 CPU0

PAX0_STATION_2_3

Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP BASEBOARD OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 42 of 155



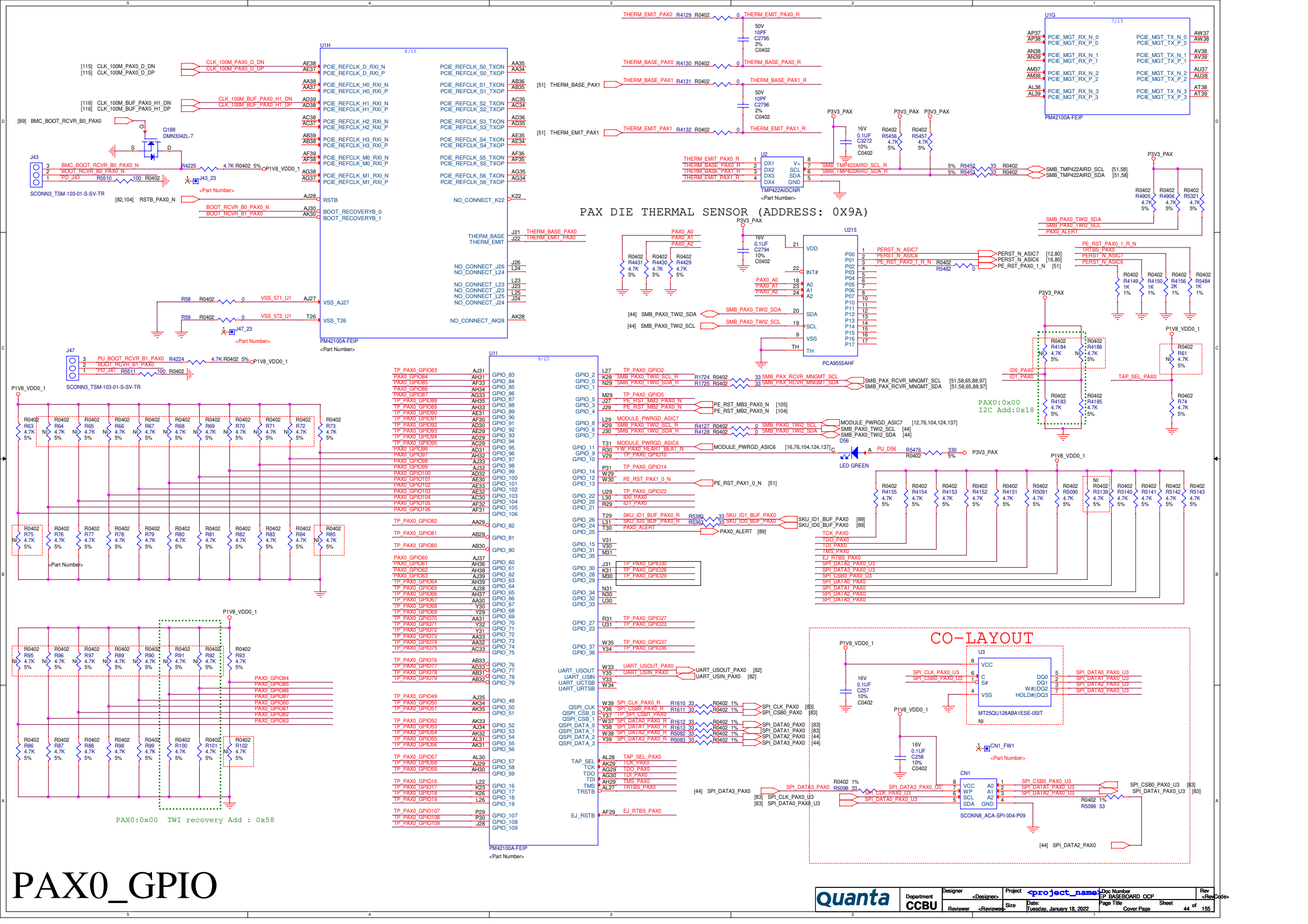
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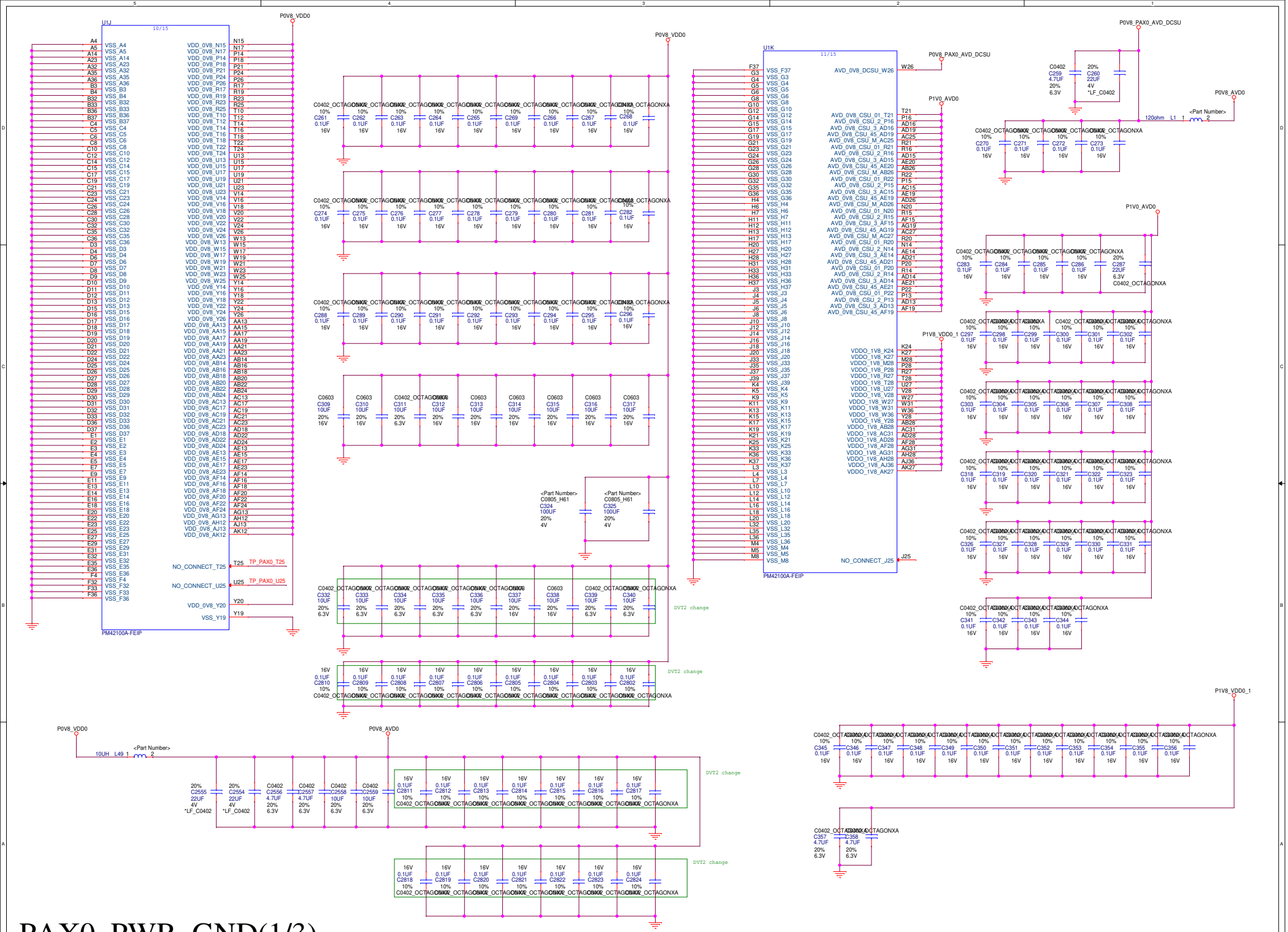


PAX 0 TO ASIC7

PAX0_STATION_4_5

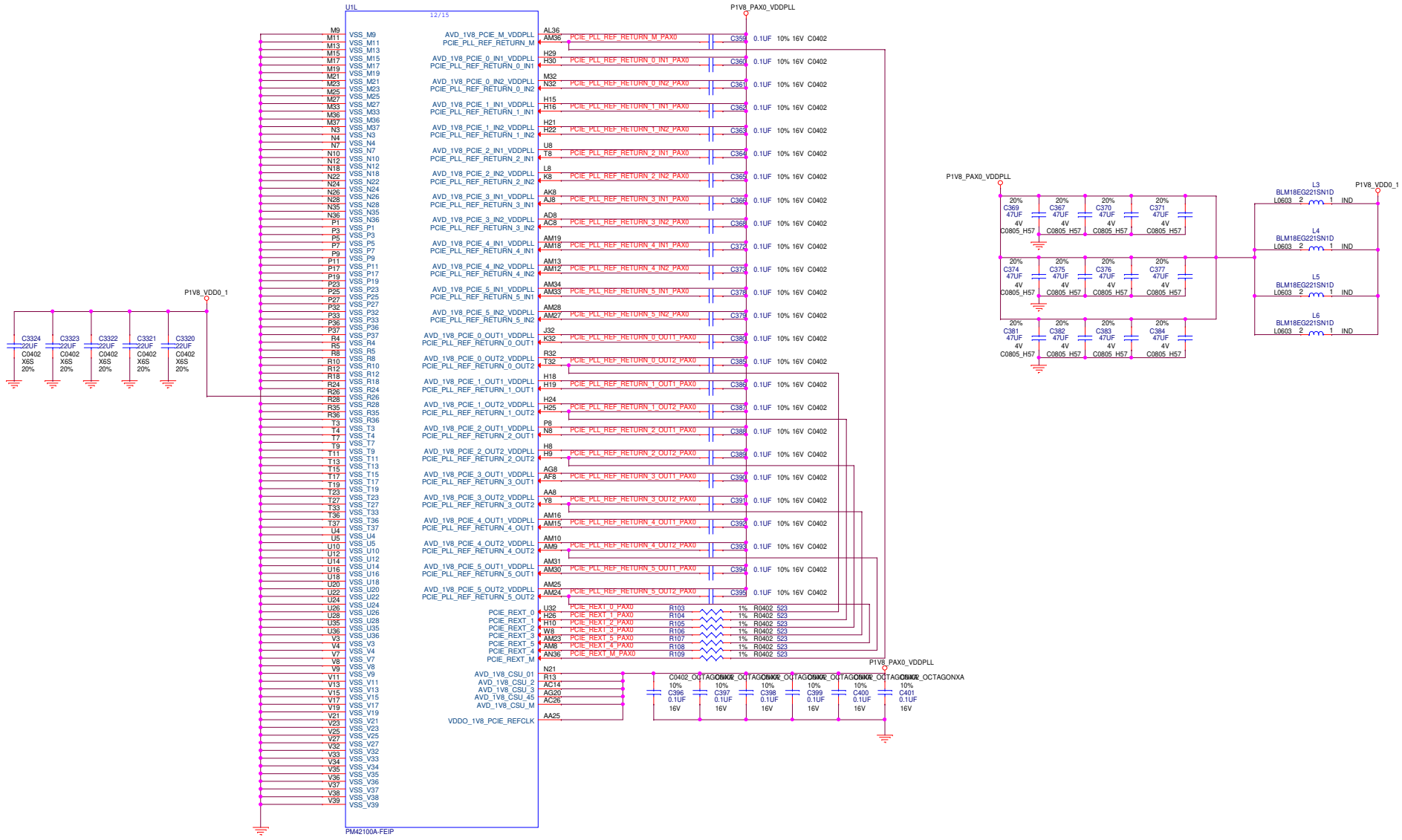
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		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 43 of 155


PAX DIE THERMAL SENSOR (ADDRESS: 0X9A)
CO-LAYOUT
PAX0:0x00 I2C Add:0x18
PAX0:0x00 TWI recovery Add : 0x58
PAX0_GPIO
U1H
U1I
U1G
U2
U215
J43
J47
Q188
DMN3042L-7
SCONN3_TSM-103-01-S-SV-TR
TMP422AIDCNR
PCA9555AHF
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MT25QU128ABA1ESE-0SIT
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LED GREEN
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Department
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Designer
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Tuesday, January 18, 2022
Doc Number
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Rev
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Cover Page
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155



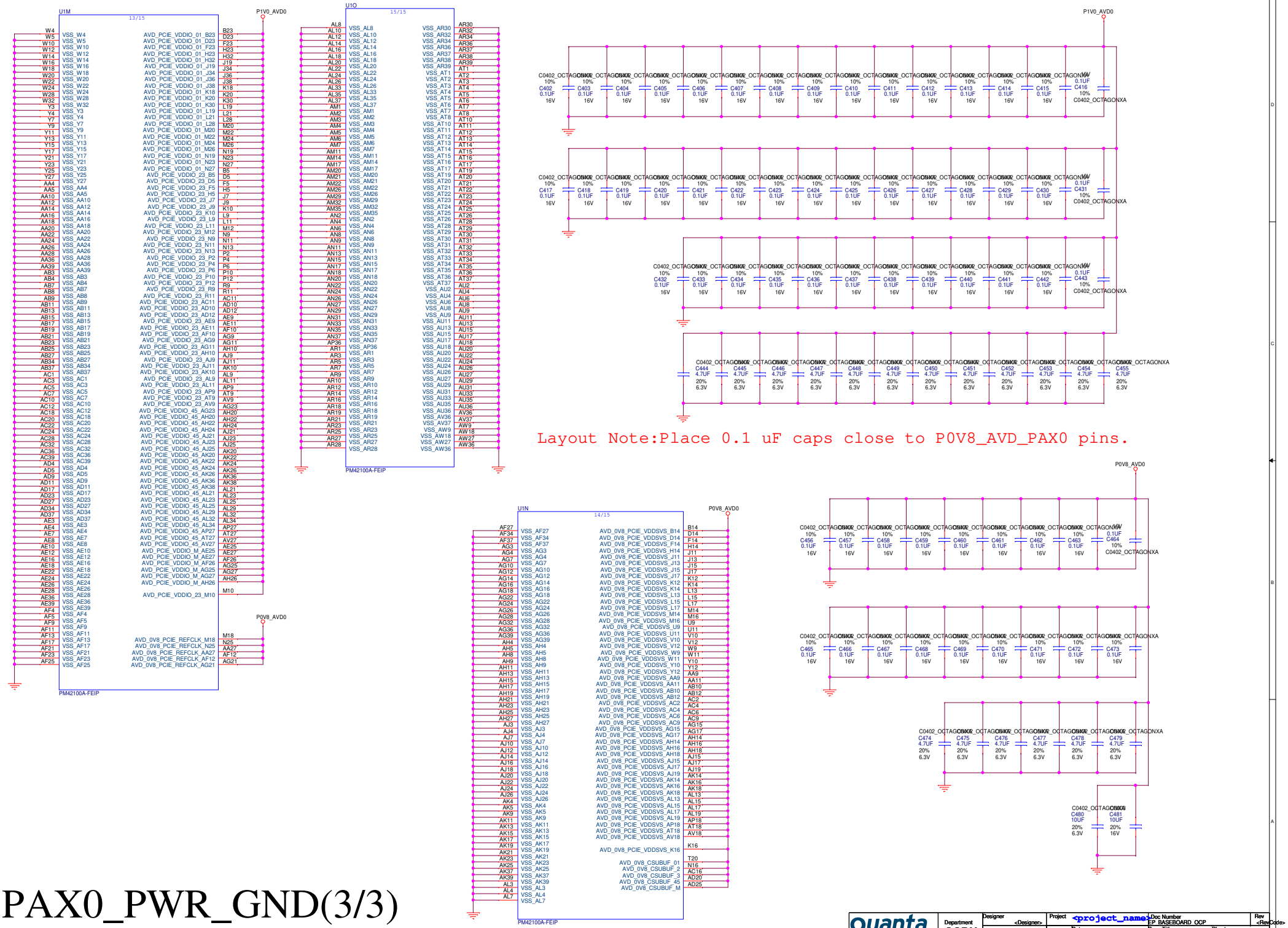
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Quanta	Department: CCBU	Designer: <Designer>	Project: <project_name>	Doc Number: EP_BASEBOARD_OCP	Rev: <RevCode>
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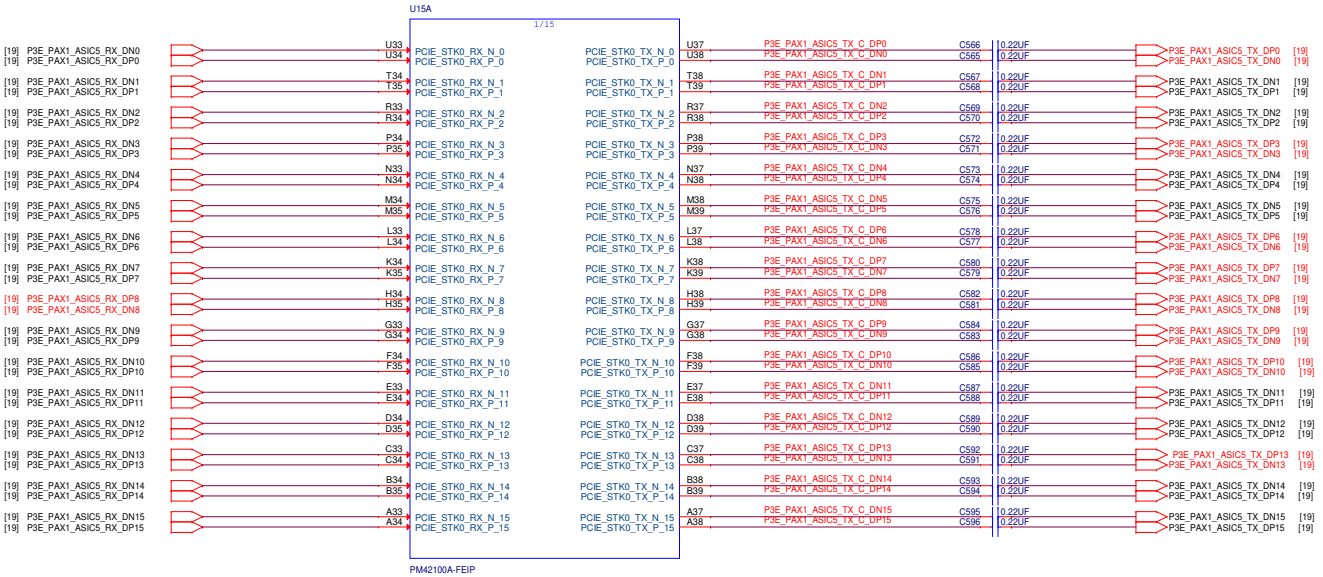
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Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 46 of 155



PAX0_PWR_GND(3/3)

Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 47 of 155

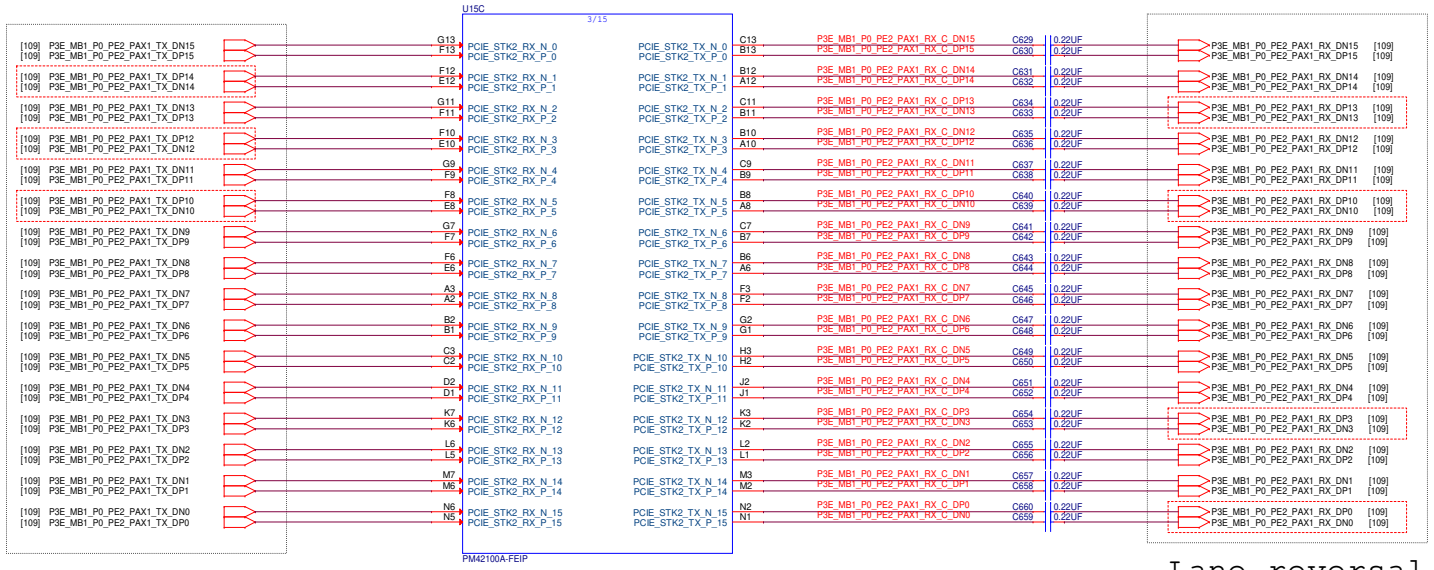


PAX1 TO ASCI5



PAX 0 TO PAX1

PAX1_STATION_0_1



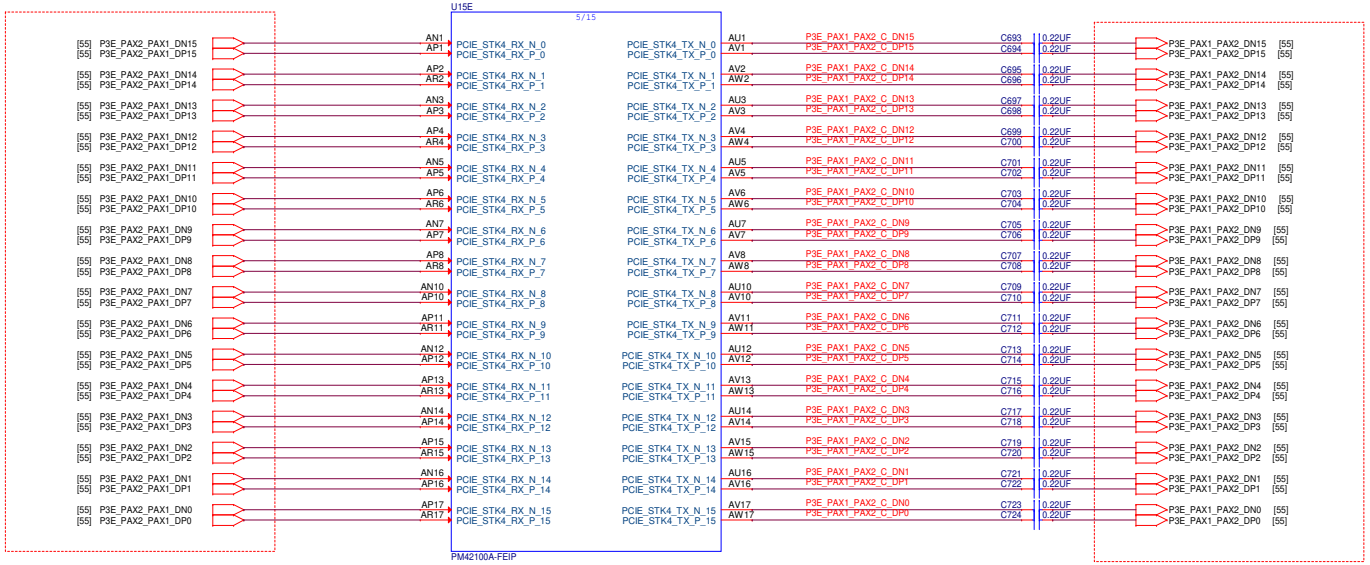
PAX1 TO "MB1" CPU0



PAX 1 TO "MB0" CPU0

PAX1_STATION_2_3

Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP BASEBOARD OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 49 of 155



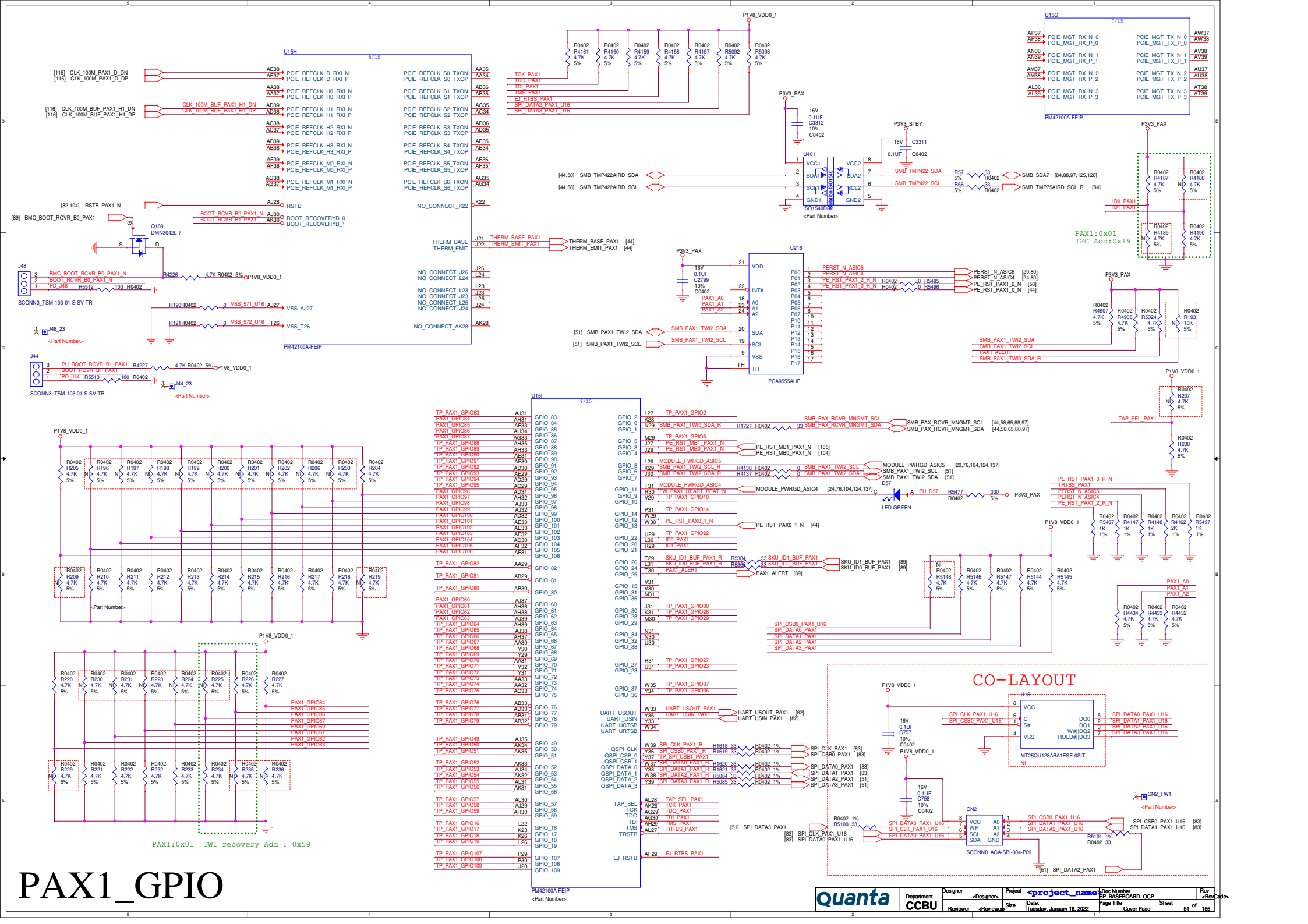
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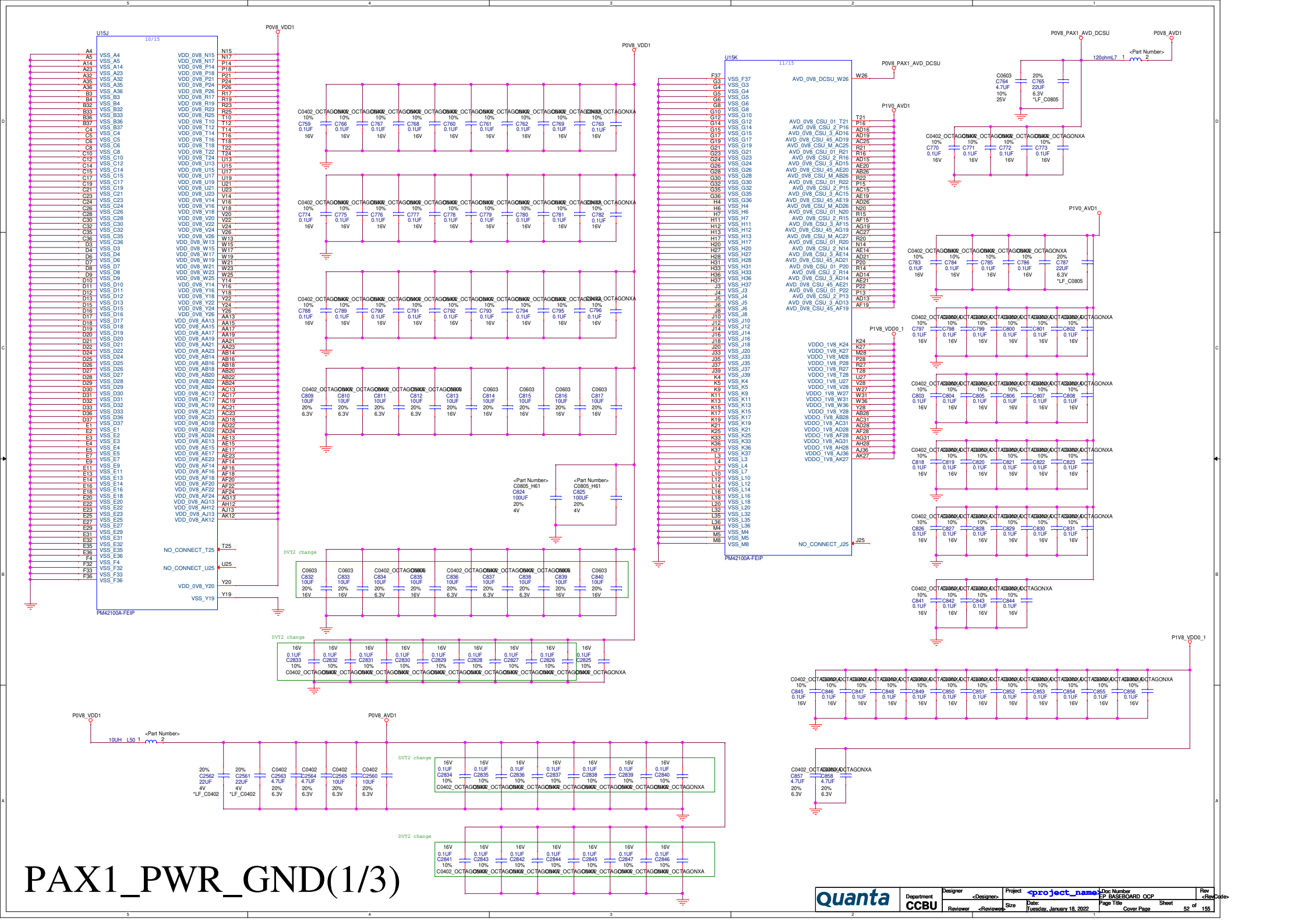


PAX 1 TO ASIC4

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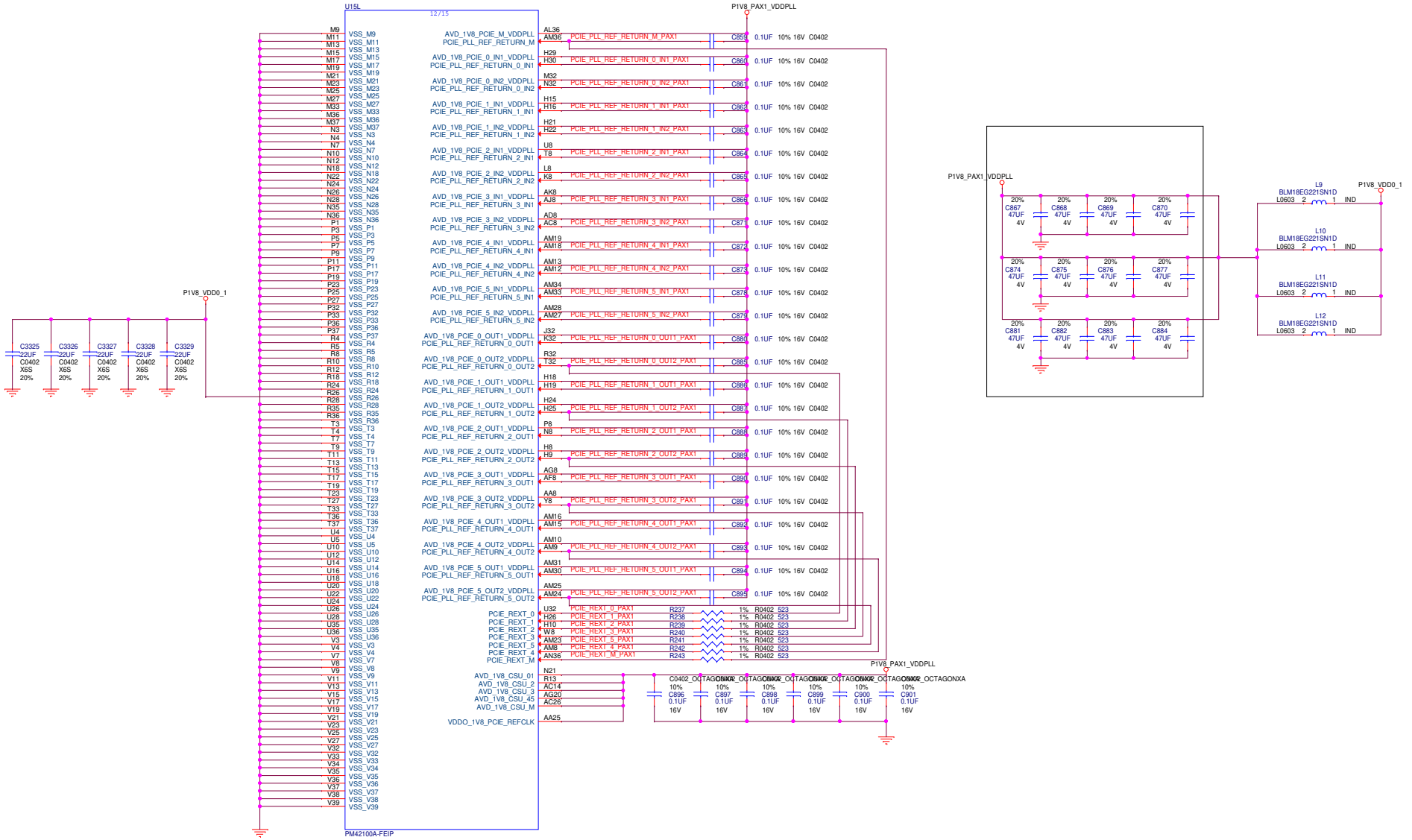
Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP BASEBOARD OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 50 of 155


U15H
8/15
PM42100A-FEIP
U15G
7/15
PM42100A-FEIP
U15I
9/15
PM42100A-FEIP
U401
ISO1540DR
U216
PCA9555AHF
Q189
DMN3042L-7
J48
J44
SCONN3_TSM-103-01-S-SV-TR
P3V3_PAX
P3V3_STBY
P1V8_VDD0_1
PAX1:0x01
I2C Add:0x19
PAX1:0x01 TWI recovery Add : 0x59
CO-LAYOUT
U16
MT25QU128ABA1ESE-0SIT
CN2
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LED GREEN
PAX1_GPIO
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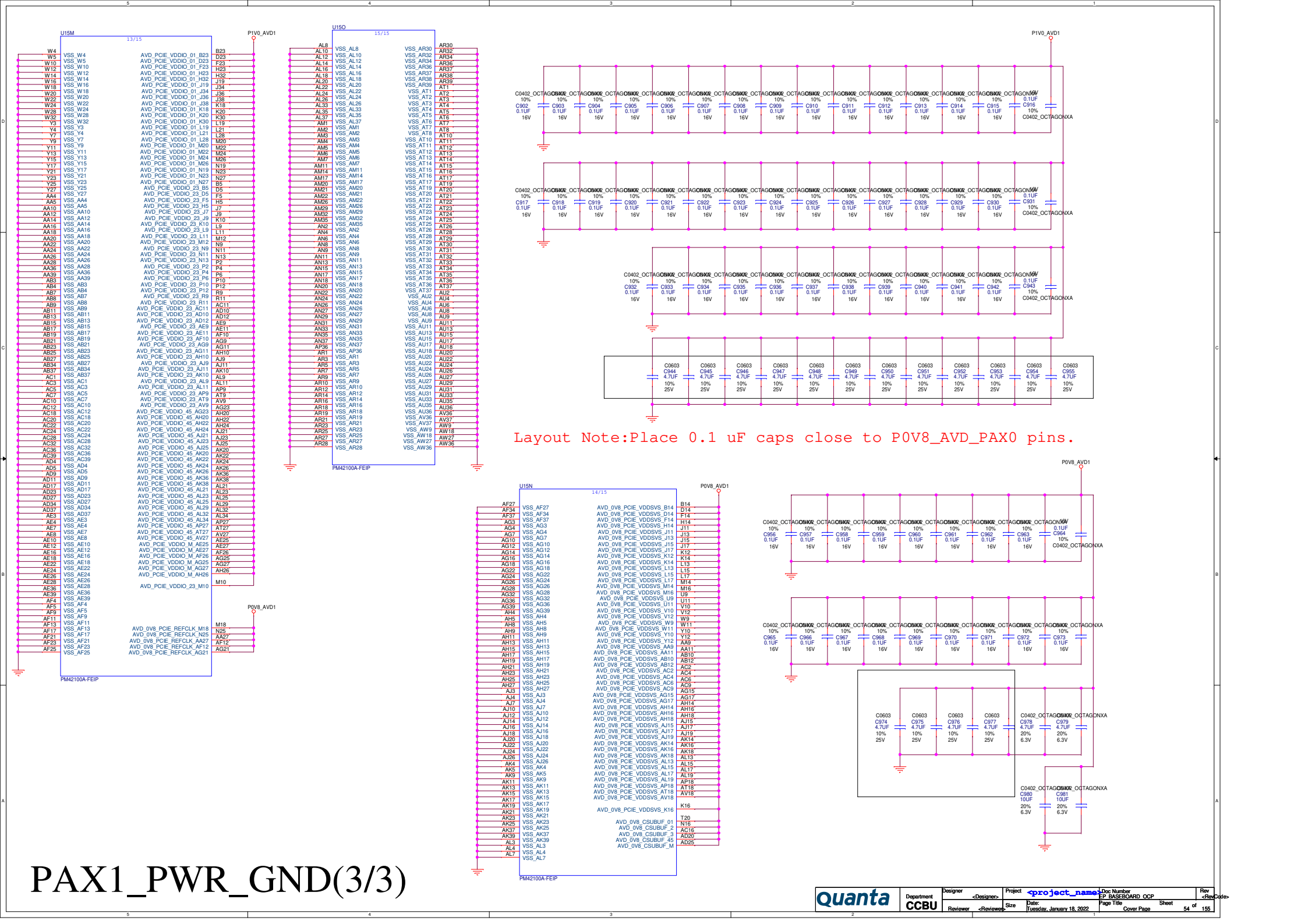
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Quanta	Department: CCBU	Designer: <Designer>	Project: <project_name>	Doc Number: EP_BASEBOARD_OCP
		Reviewer: <Reviewer>	Size	Date: Tuesday, January 18, 2022
				Page Title: Cover Page
				Rev: <RevCode>
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PAX1_PWR_GND(2/3)

Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 53 of 155

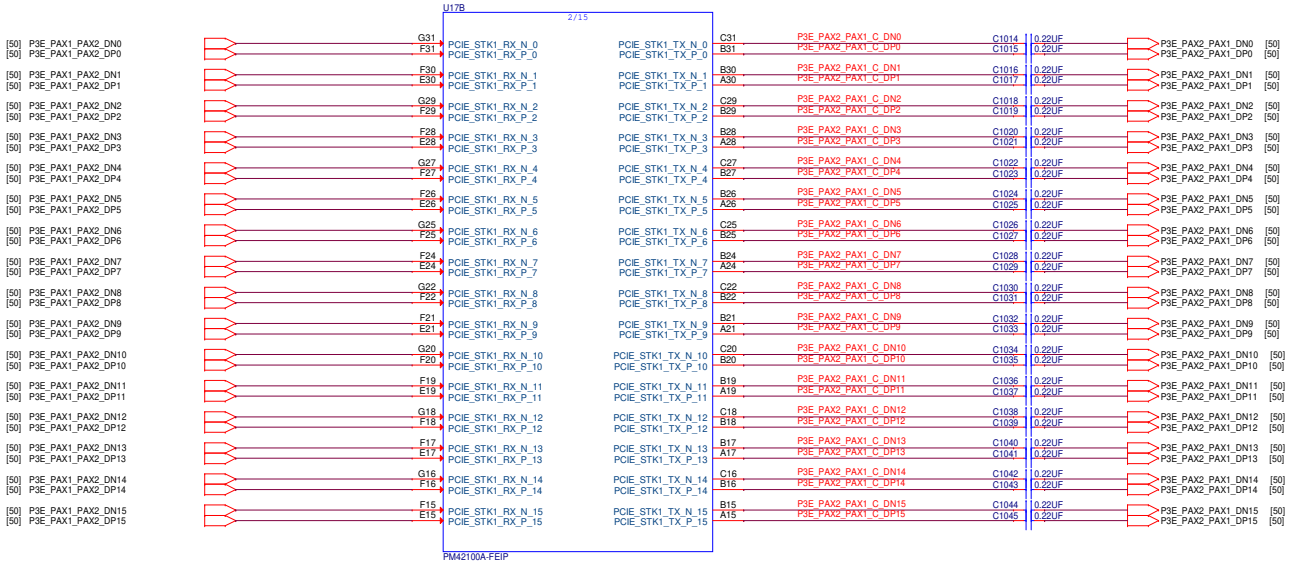


PAX1_PWR_GND(3/3)

Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 54 of 155



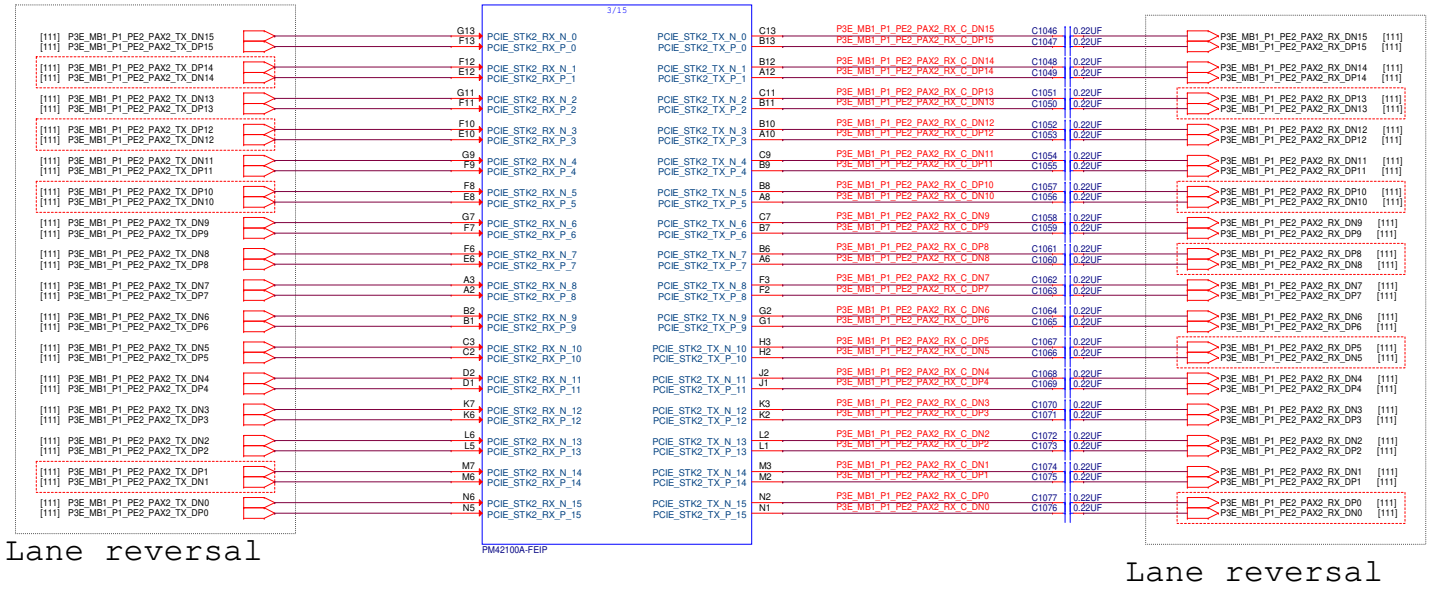
PAX2 TO ASCI2



PAX 2 TO PAX1

PAX2_STATION_0_1

Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP BASEBOARD OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 55 of 155



PAX 2 TO "MB1" CPU1



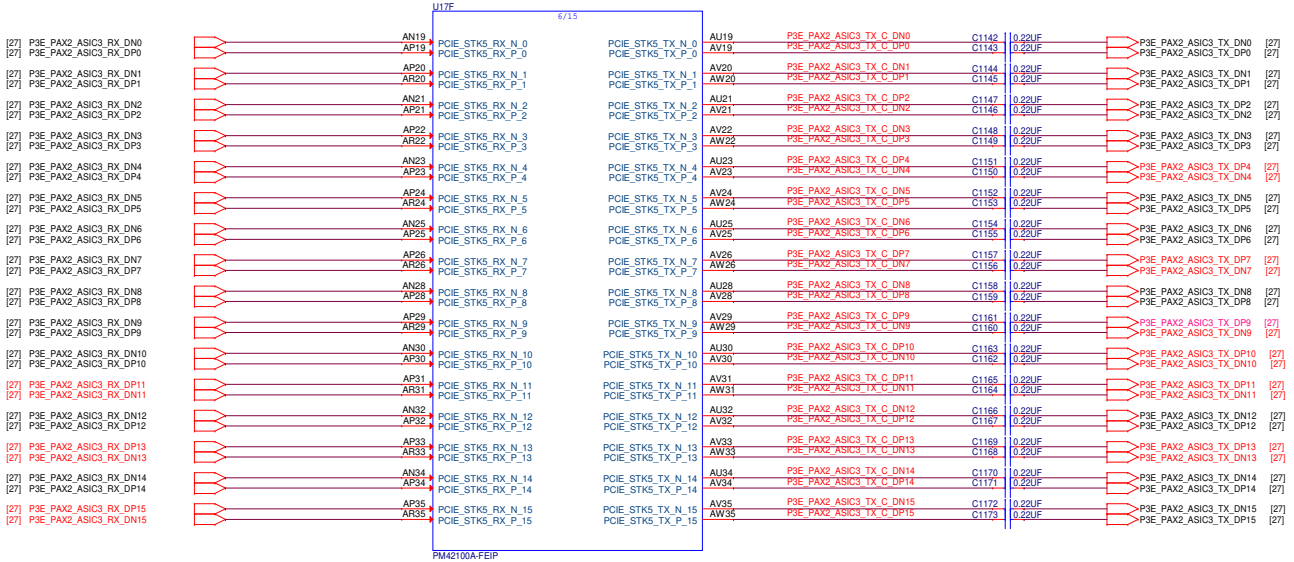
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PAX2_STATION_2_3

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		Reviewer: <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title: Cover Page — Sheet 56 of 155



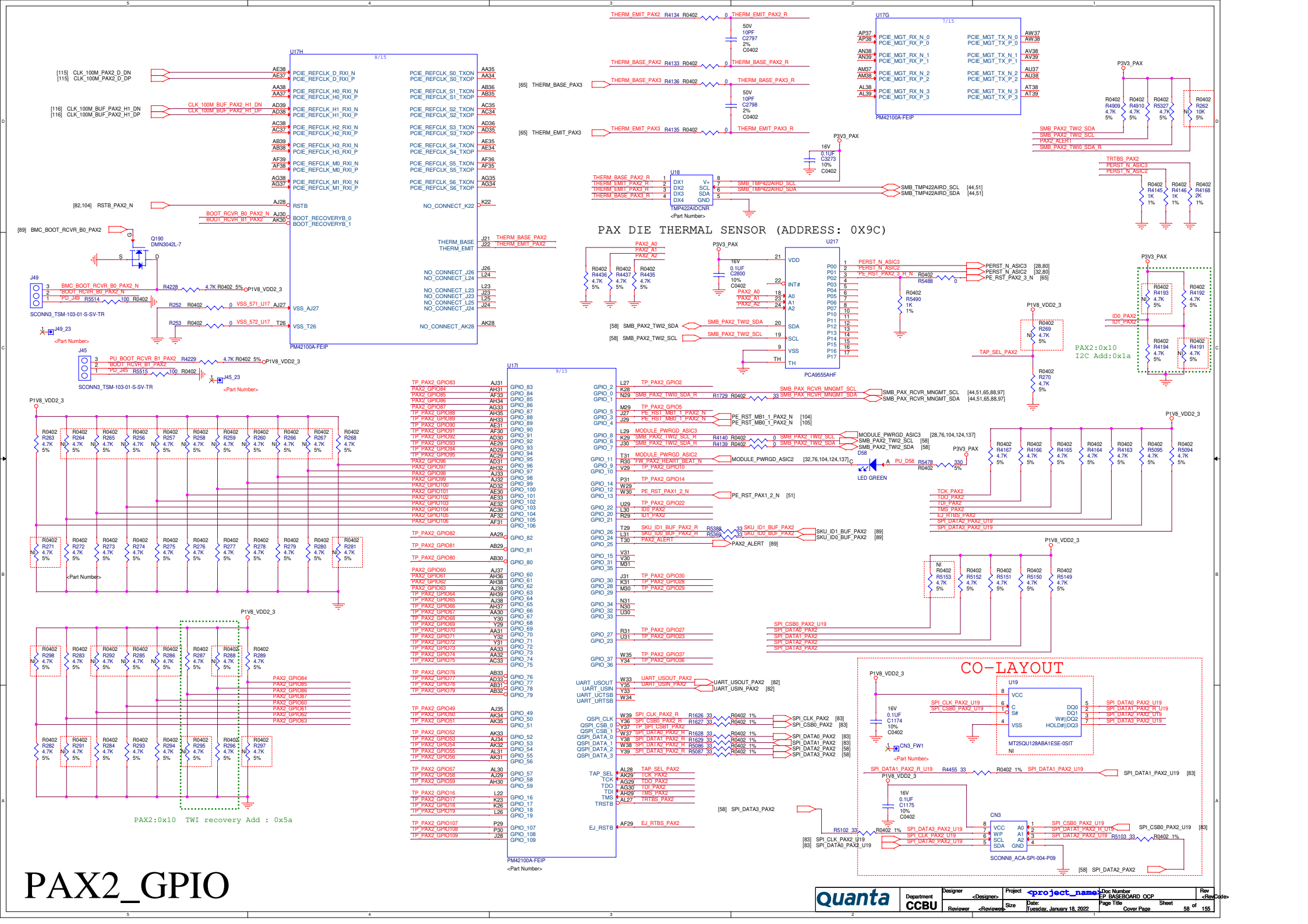
PAX2 TO PAX3

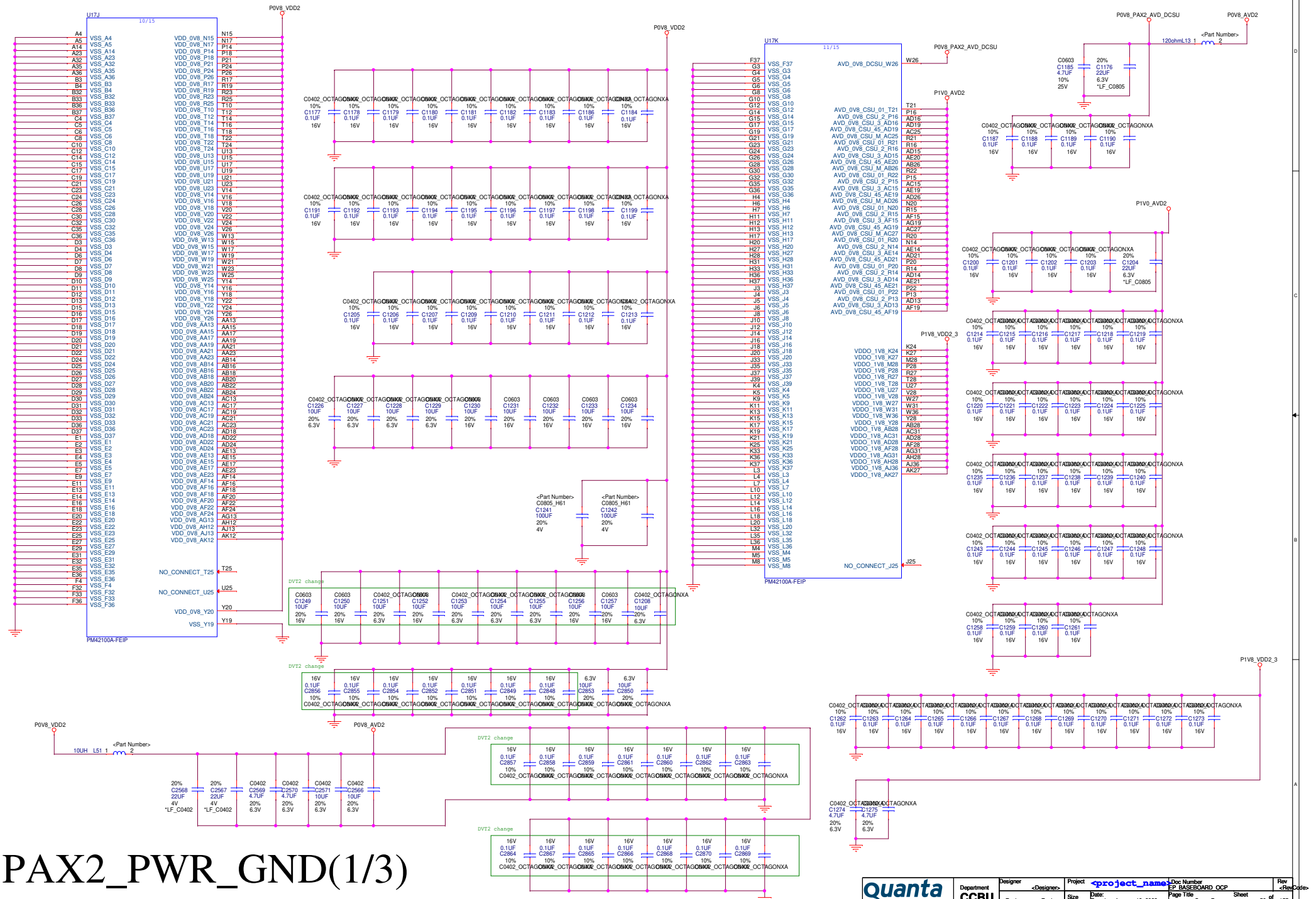


PAX 2 TO ASIC3

PAX2_STATION_4_5

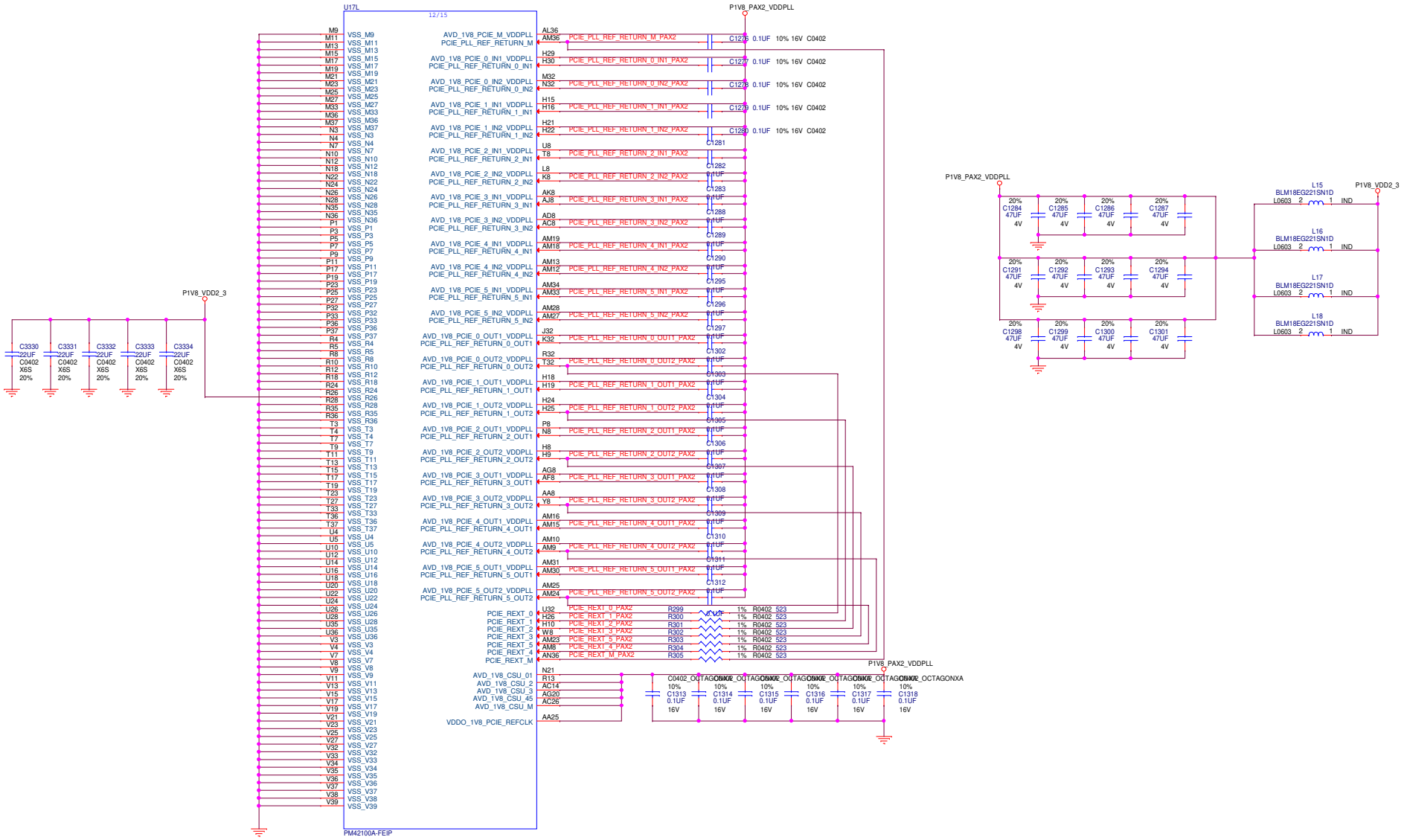
Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP BASEBOARD OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 57 of 155


PAX DIE THERMAL SENSOR (ADDRESS: 0X9C)
CO-LAYOUT
PAX2:0x10 I2C Add:0x1a
PAX2:0x10 TWI recovery Add : 0x5a
PAX2_GPIO
U17H
U17I
U17G
U18
U217
PM42100A-FEIP
TMP422AIDCNR
PCA9555AHF
MT25QU128ABA1ESE-0SIT
SCONN8_ACA-SPI-004-P09
SCONN3_TSM-103-01-S-SV-TR
Q190 DMN3042L-7
LED GREEN
P3V3_PAX
P1V8_VDD2_3
Quanta
Department CCBU
Designer <Designer>
Reviewer <Reviewer>
Project <project_name>
Size
Date: Tuesday, January 18, 2022
Doc Number EP_BASEBOARD_OCP
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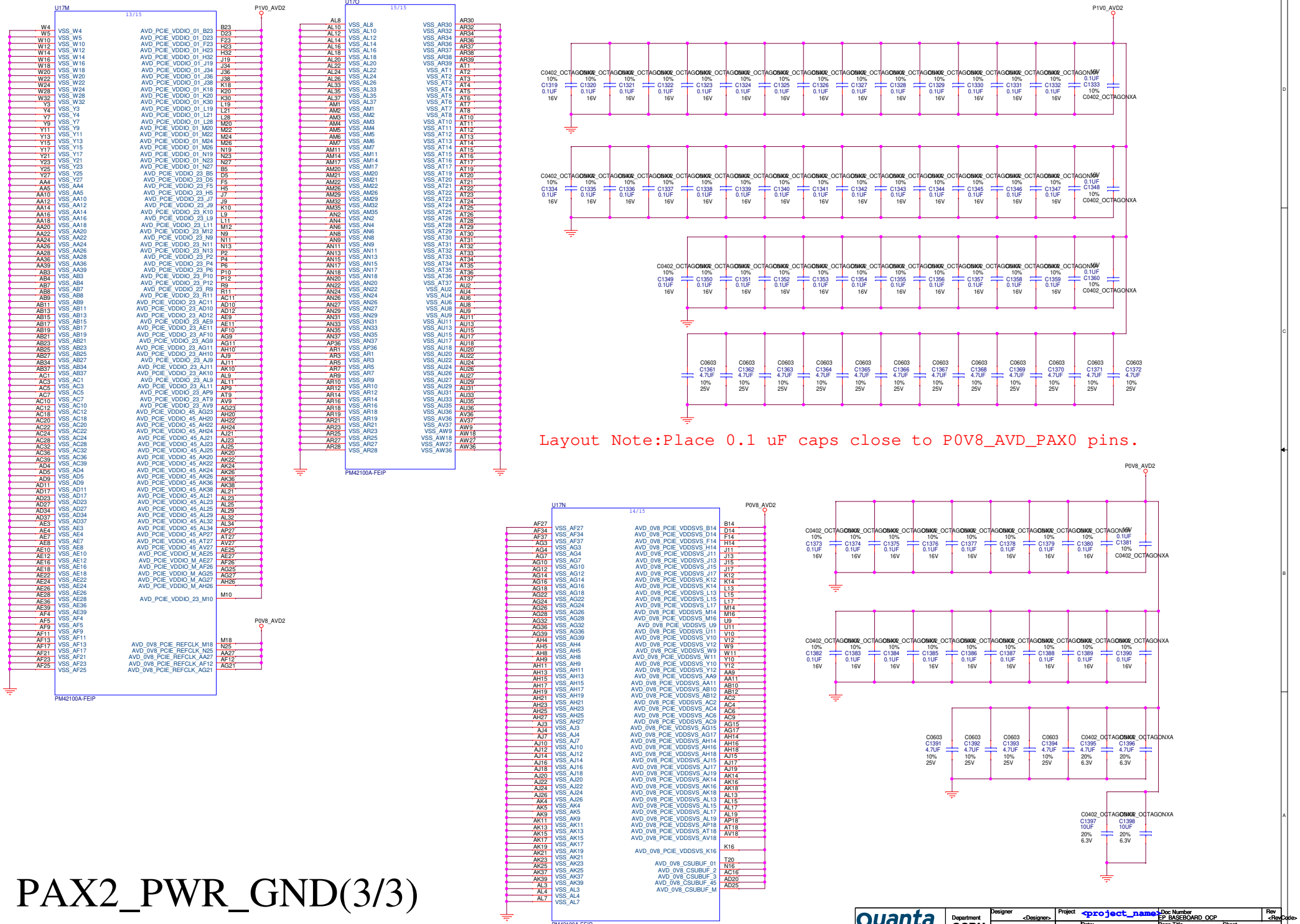
PAX2_PWR_GND(1/3)

Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP BASEBOARD OCP
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022
				Page Title Cover Page
				Rev <RevCode>
				Sheet 59 of 155



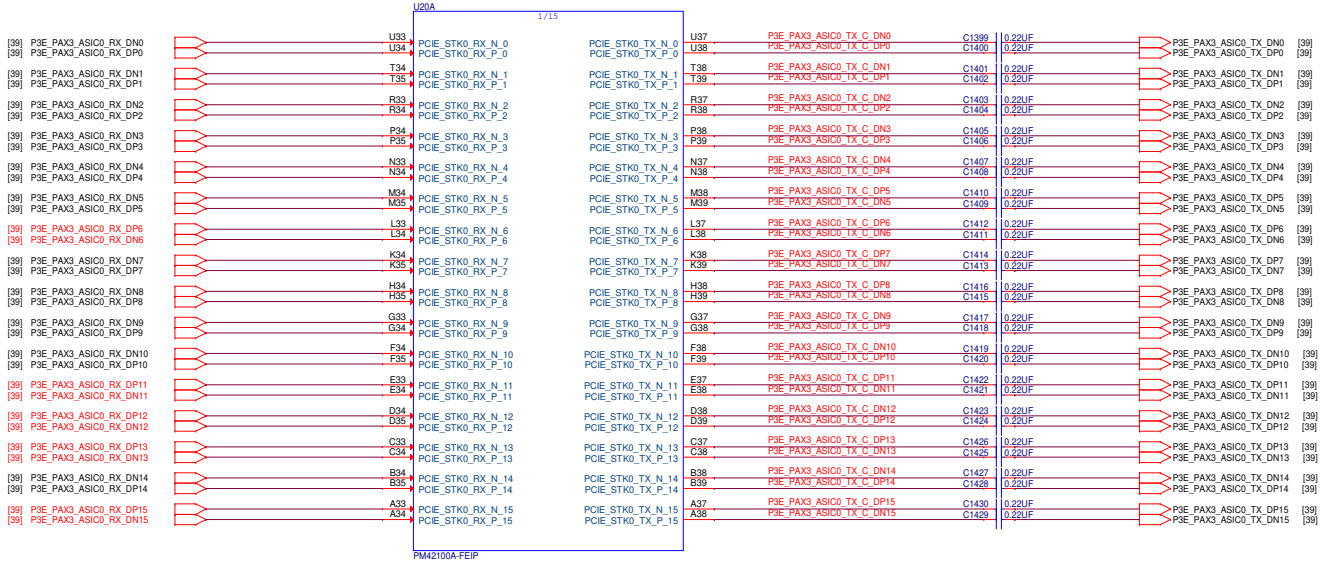
PAX2_PWR_GND(2/3)

Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 60 of 155

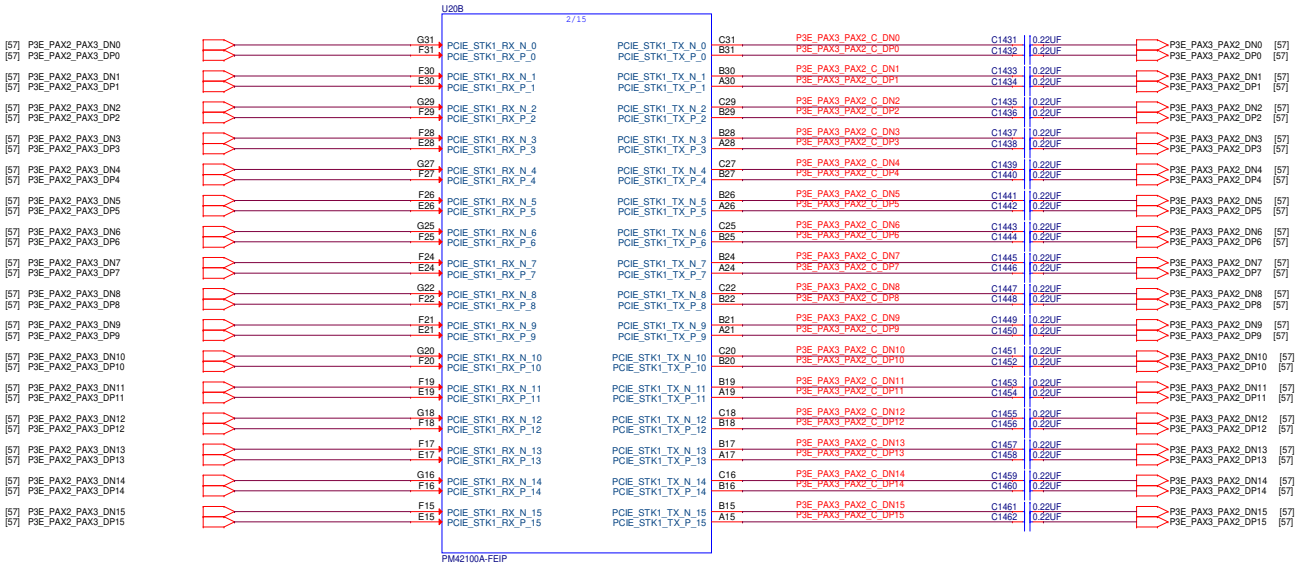


PAX2_PWR_GND(3/3)

Quanta	Department: CCBU	Designer: <Designer>	Project: <project_name>
		Reviewer: <Reviewer>	Size
Doc Number: EP_BASEBOARD_OCP	Rev: <RevCode>	Page Title: Cover Page	Sheet 61 of 155
Date: Tuesday, January 18, 2022			



PAX3 TO ASIC0



PAX 3 TO PAX2

PAX3_STATION_0_1

Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 62 of 155



PAX3 TO "MB3" CPU1

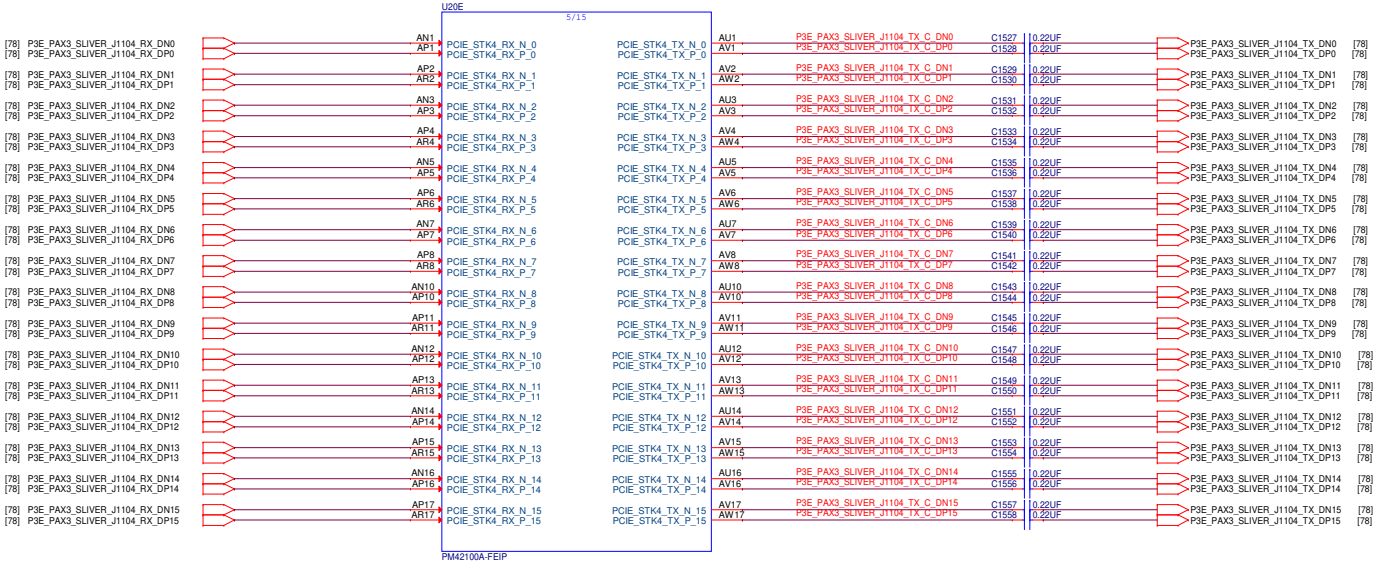


PAX 3 TO MB2 CPU1

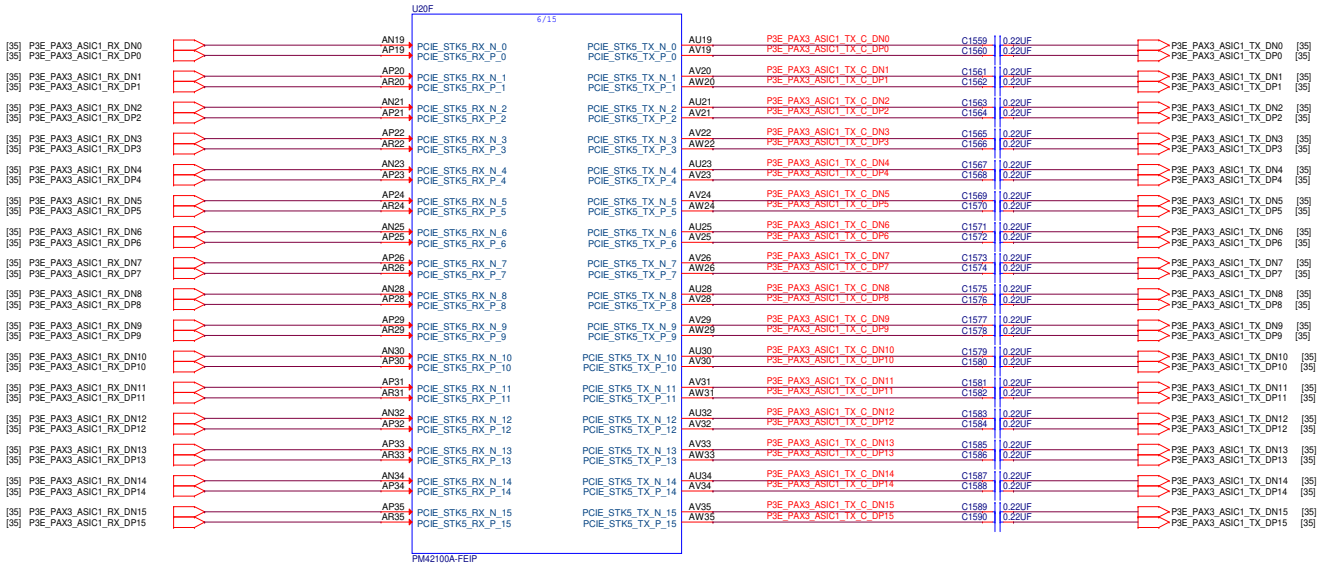
PN SWAP

PAX3_STATION_2_3

Quanta	Department: CCBU	Designer: <Designer>	Project: <project_name>	Doc Number: EP BASEBOARD OCP	Rev: <RevCode>
		Reviewer: <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title: Cover Page — Sheet 63 of 155



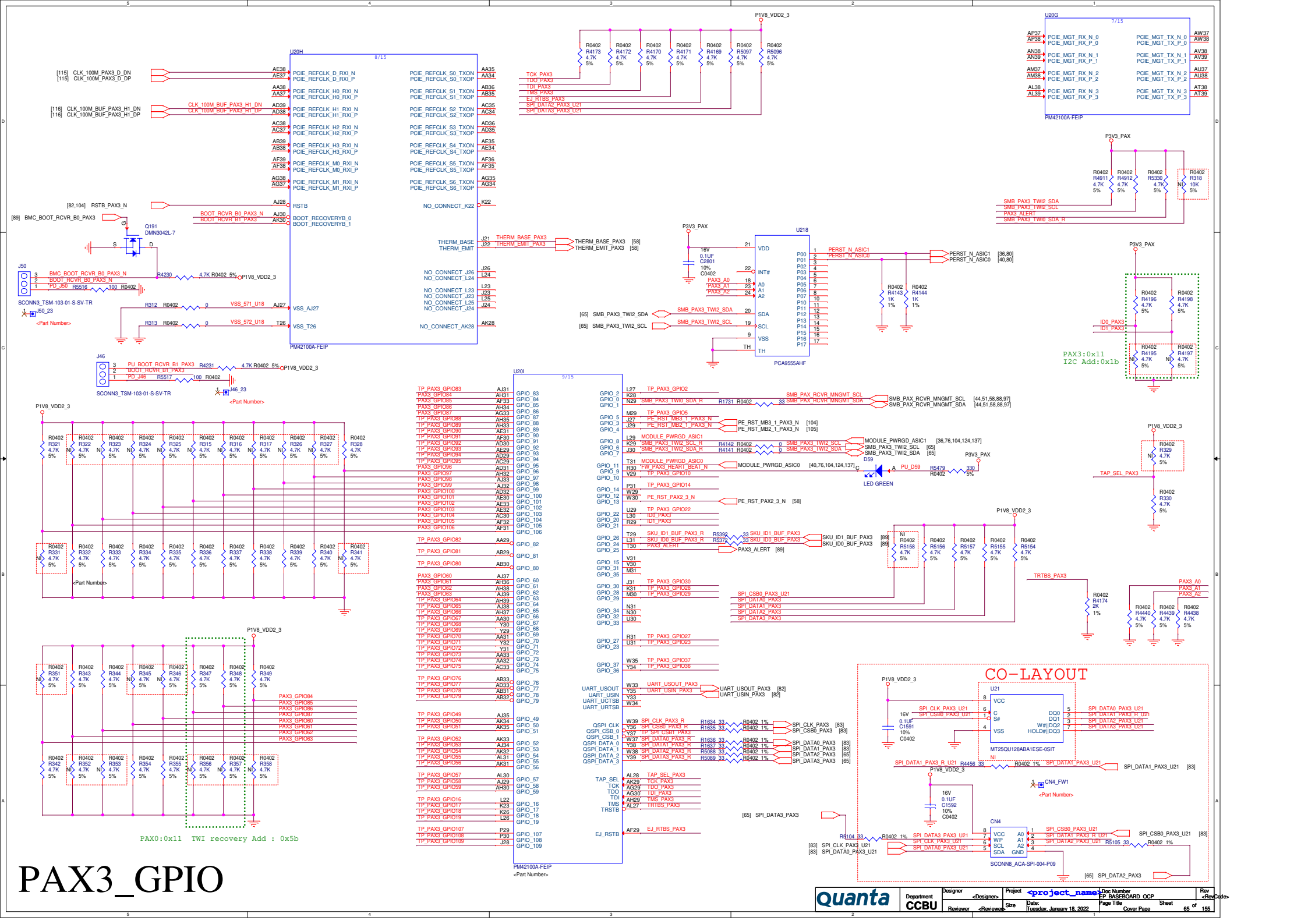
PAX3 TO DEBUG AND BMC

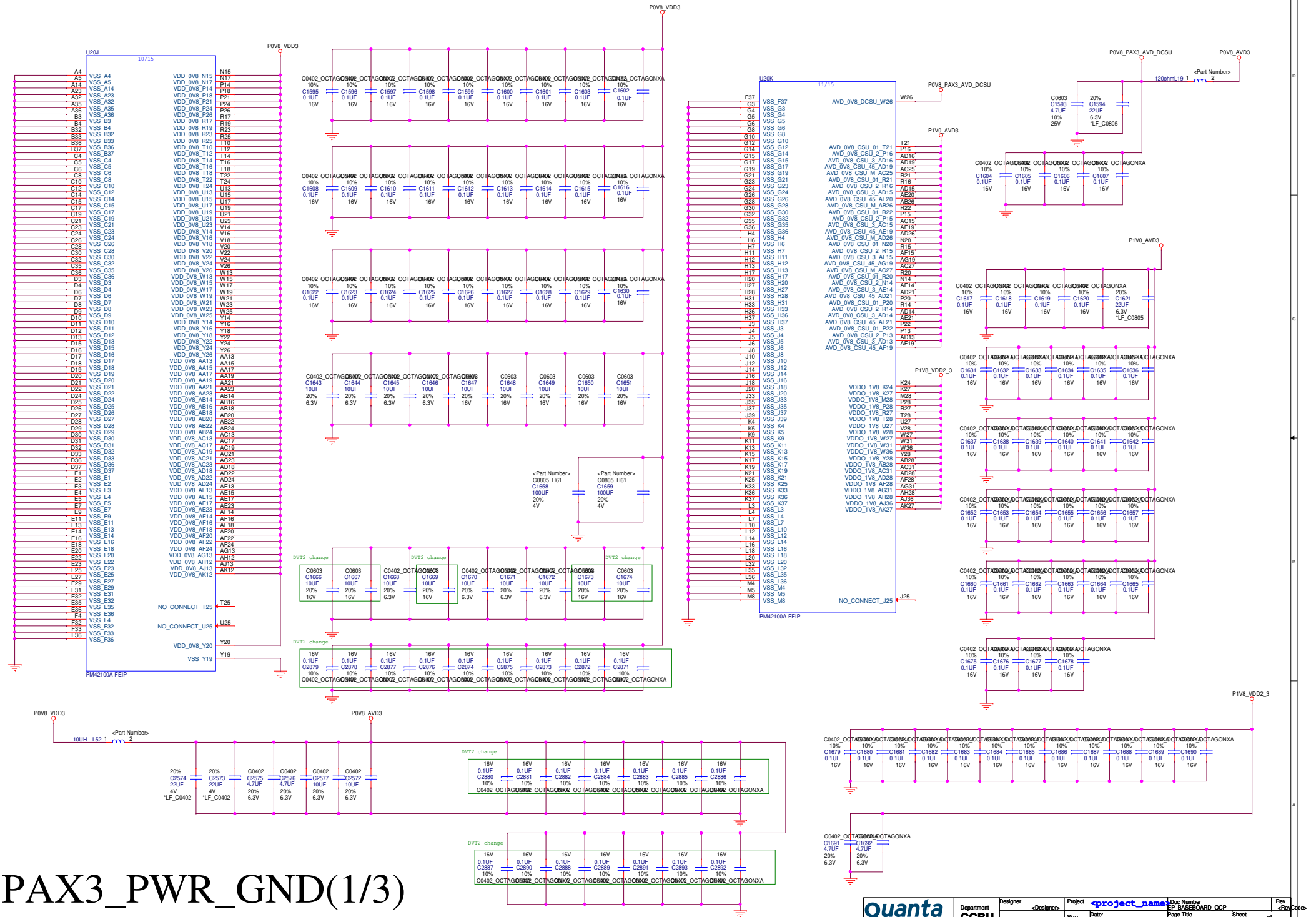


PAX 3 TO ASIC1

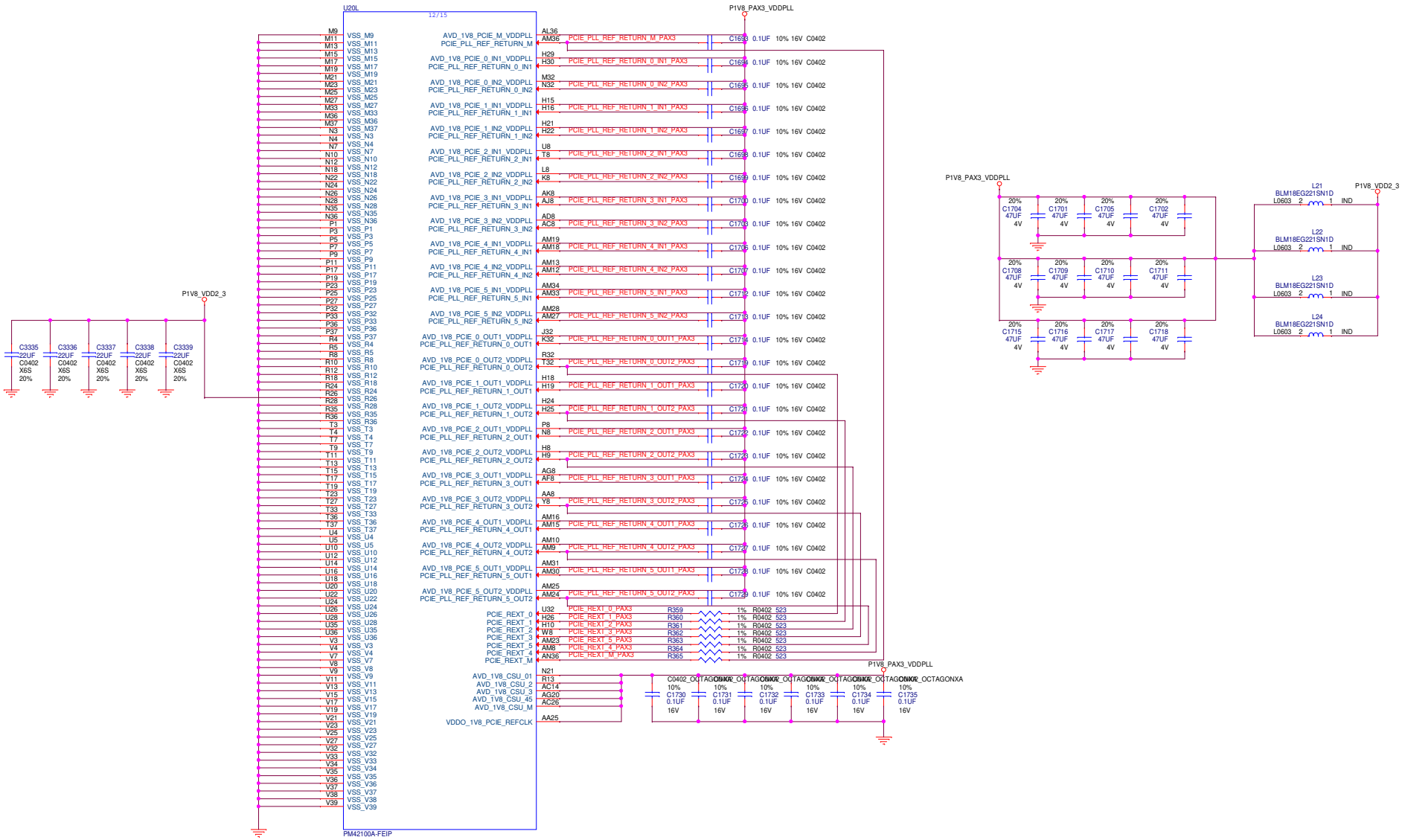
PAX3_STATION_4_5

Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 64 of 155


U20H
8/15
PM42100A-FEIP
U20I
9/15
PM42100A-FEIP
U20G
7/15
PM42100A-FEIP
U218
PCA9555AHF
Q191
DMN3042L-7
J50
SCONN3_TSM-103-01-S-SV-TR
J46
SCONN3_TSM-103-01-S-SV-TR
U21
MT25QU128ABA1ESE-0SIT
CN4
SCONN8_ACA-SPI-004-P09
CN4_FW1
D59
LED GREEN
P1V8_VDD2_3
P3V3_PAX
PAX0:0x11 TWI recovery Add : 0x5b
PAX3:0x11
I2C Add:0x1b
CO-LAYOUT
PAX3_GPIO
Quanta
Department
CCBU
Designer
<Designer>
Reviewer
<Reviewer>
Project
<project_name>
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Date: Tuesday, January 18, 2022
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155

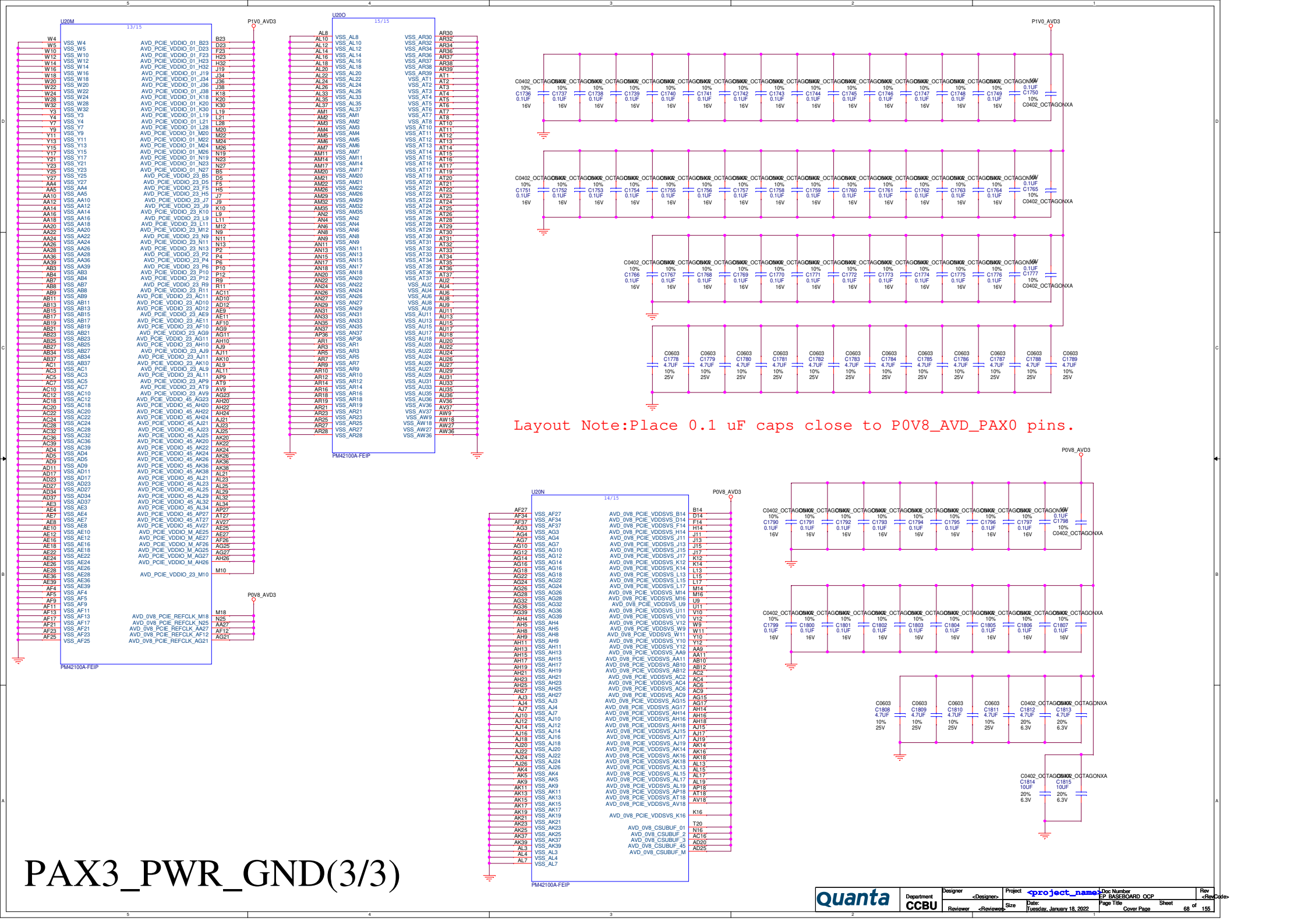


Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 66 of 155



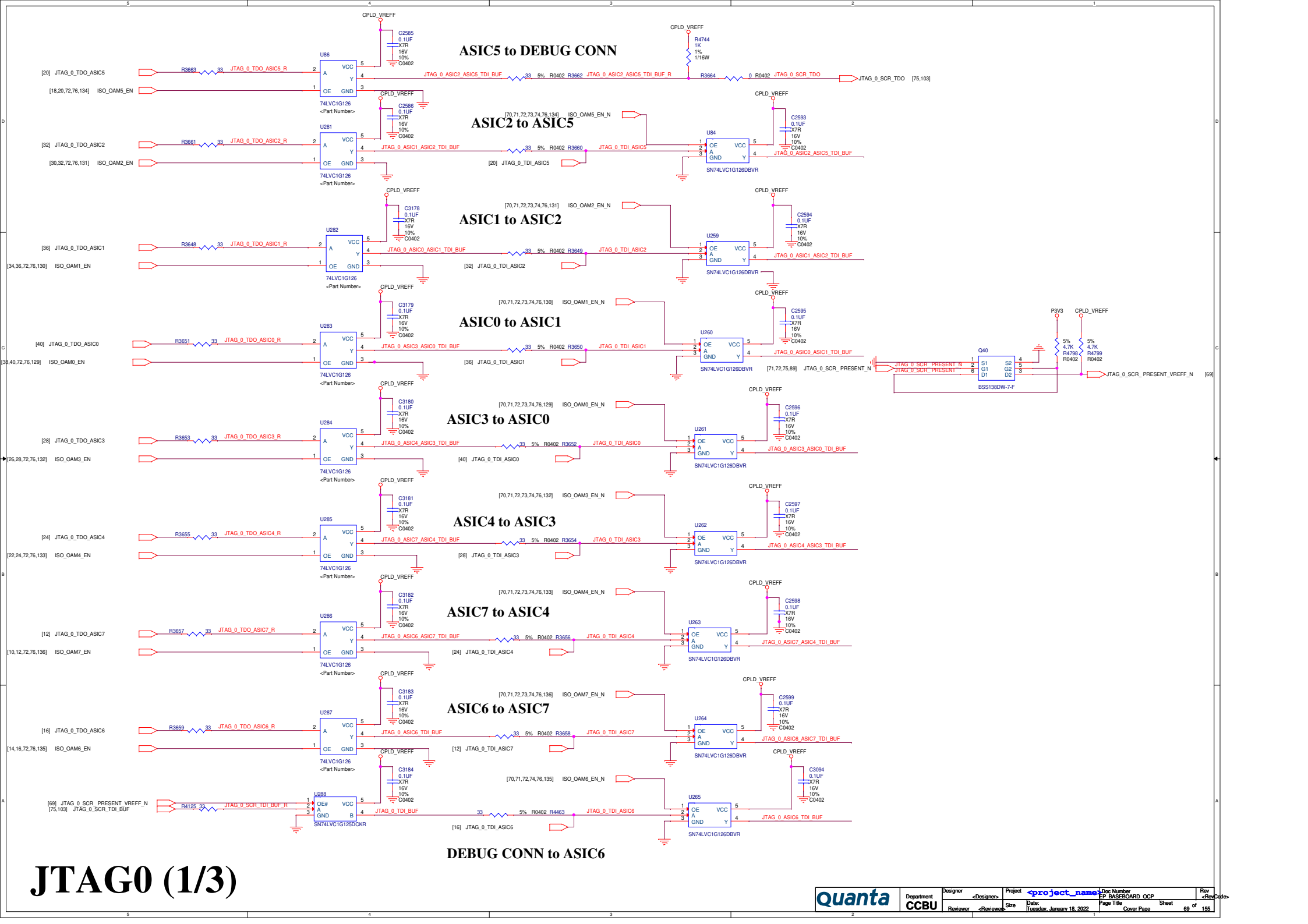
PAX3_PWR_GND(2/3)

Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 67 of 155



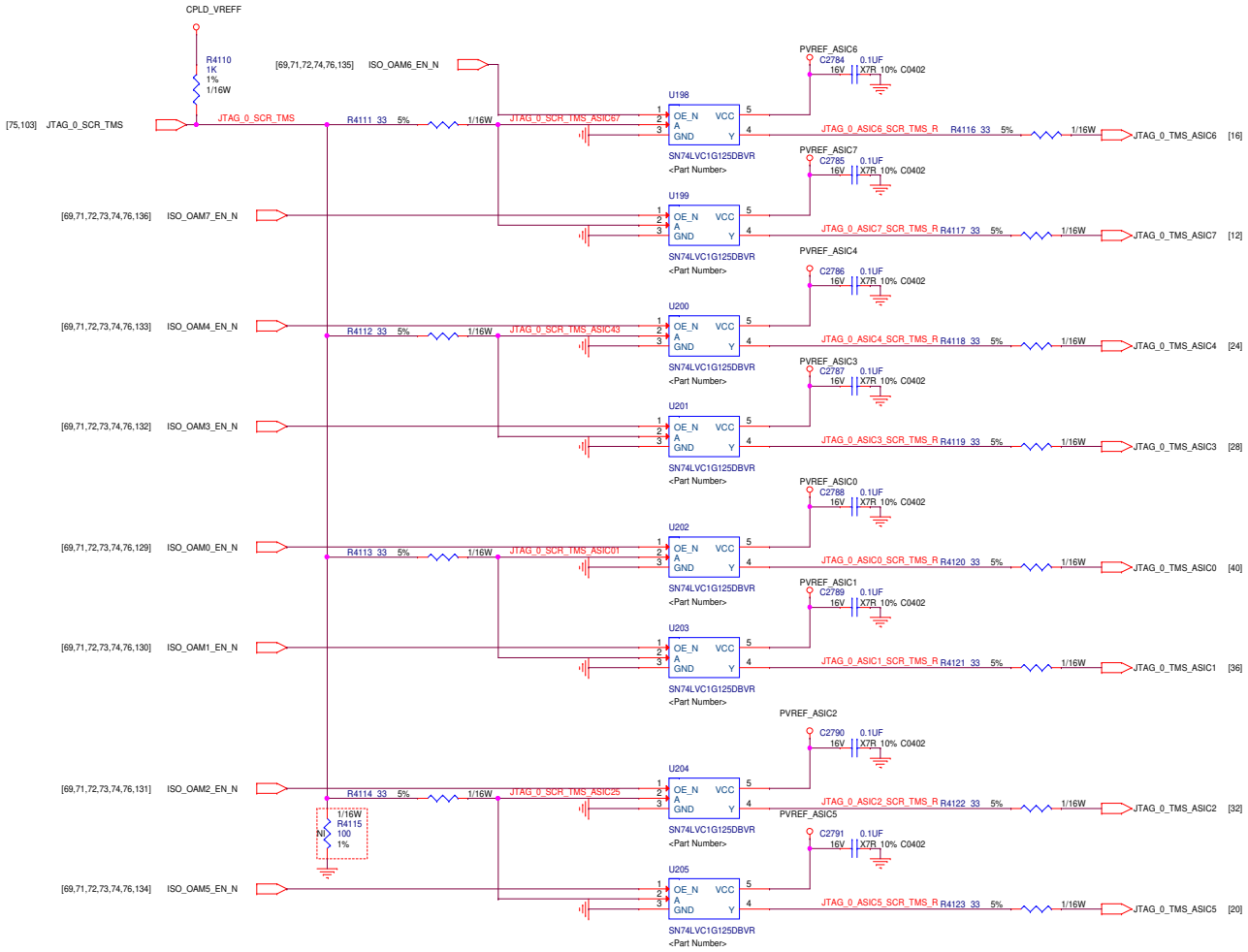
PAX3_PWR_GND(3/3)

Quanta	Department: CCBU	Designer: <Designer>	Project: <project_name>
		Reviewer: <Reviewer>	Size
		Date: Tuesday, January 18, 2022	Doc Number: EP BASEBOARD_OCP
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		Sheet 68 of 155	



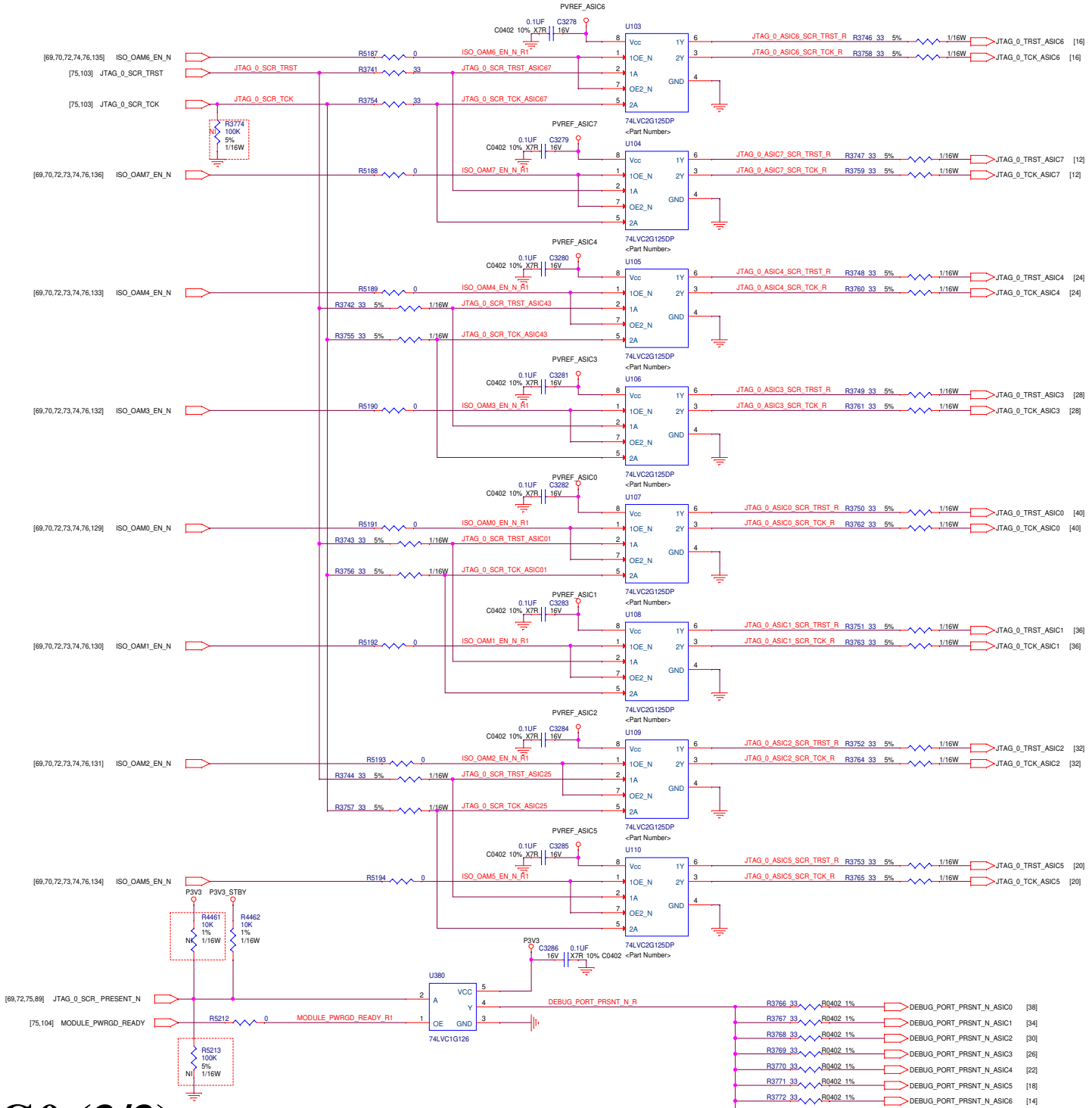
JTAG0 (1/3)

Quanta	Department: CCBU	Designer: <Designer>	Project: <project_name>
		Reviewer: <Reviewer>	Size
		Date: Tuesday, January 18, 2022	Sheet 69 of 155
Doc Number: EP_BASEBOARD_OCP	Rev: <RevCode>	Page Title: Cover Page	



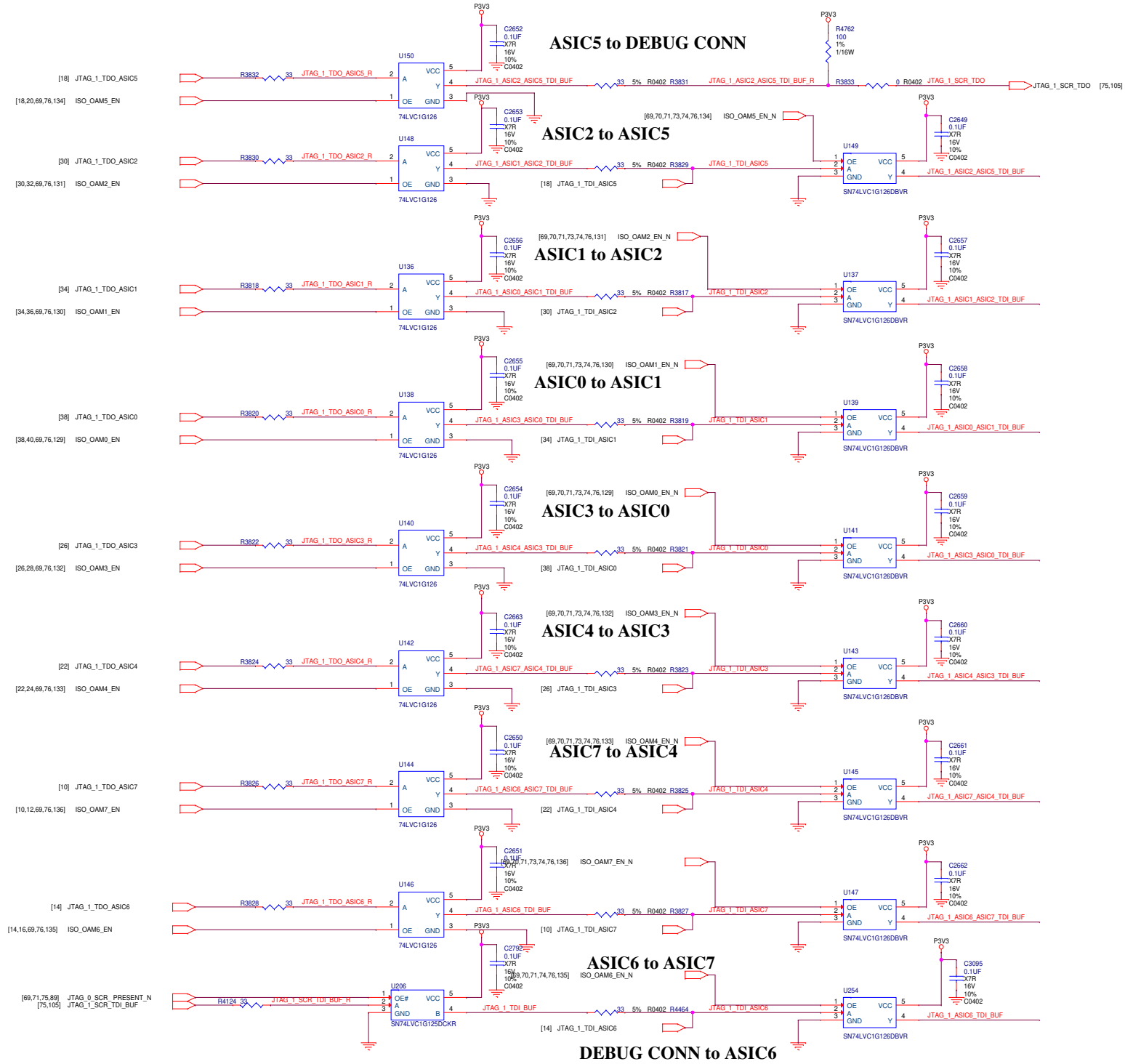
JTAG0 (2/3)

Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 70 of 155



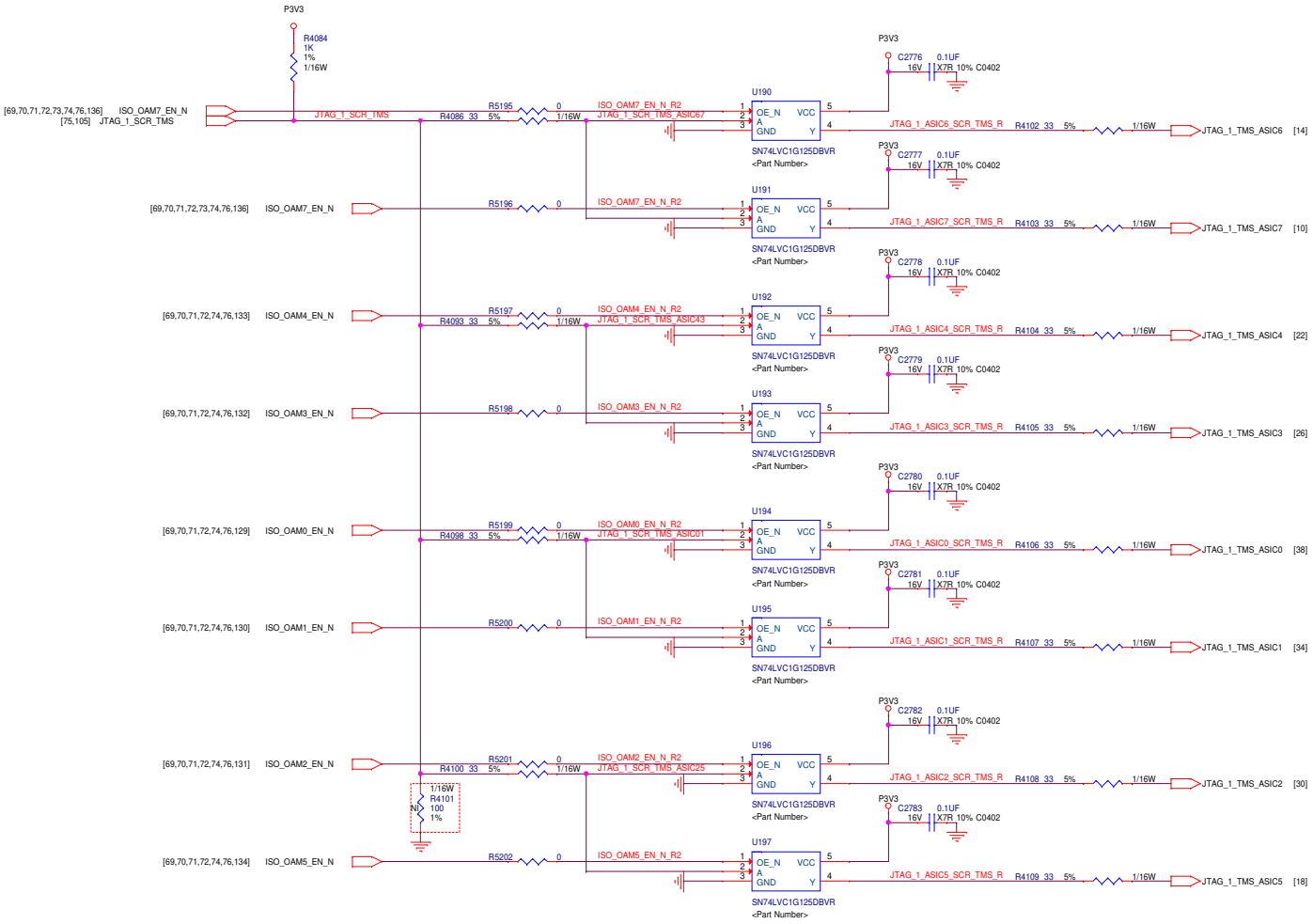
JTAG0 (3/3)

Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP BASEBOARD OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 71 of 155



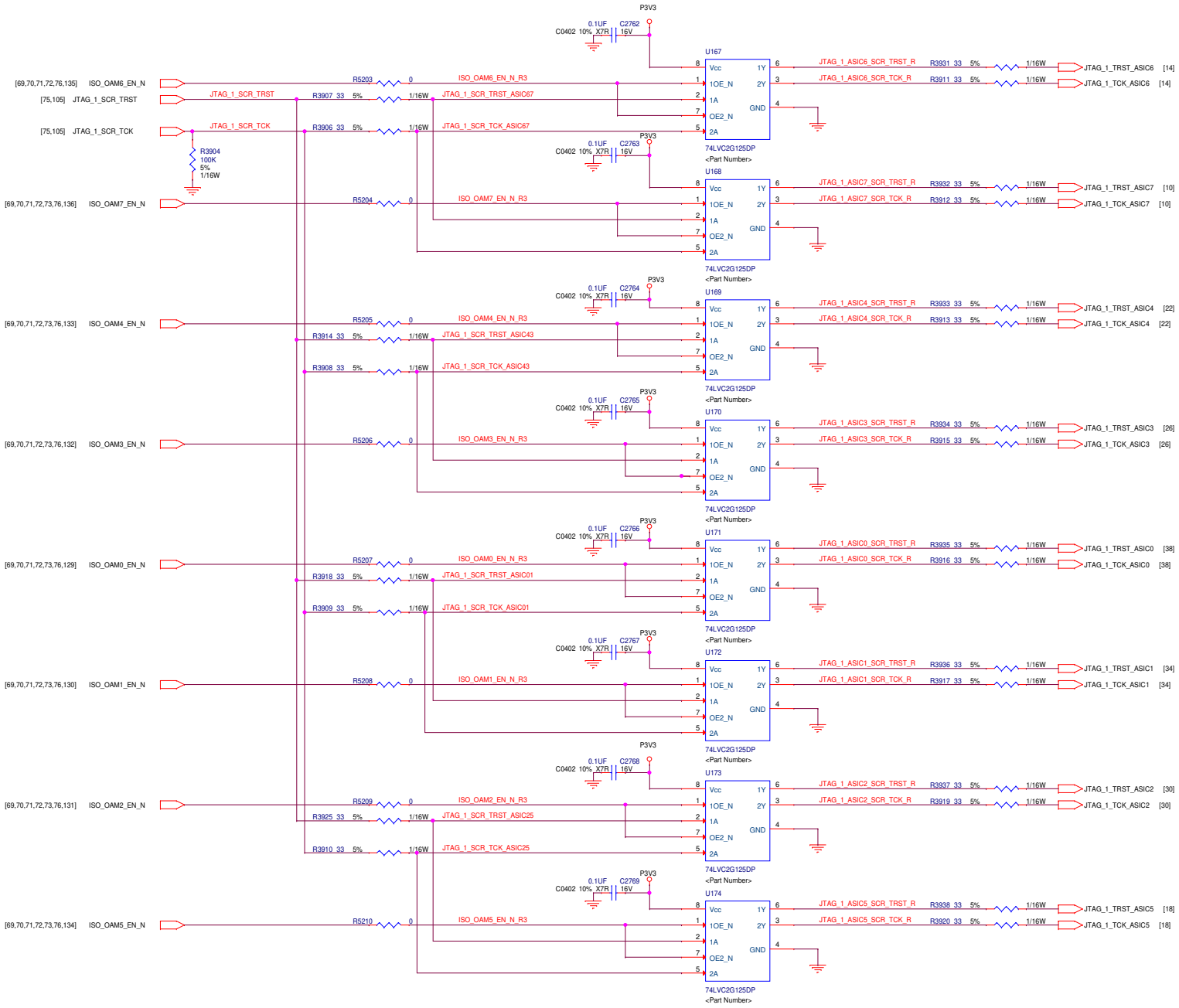
JTAG1 (1/3)

Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 72 of 155



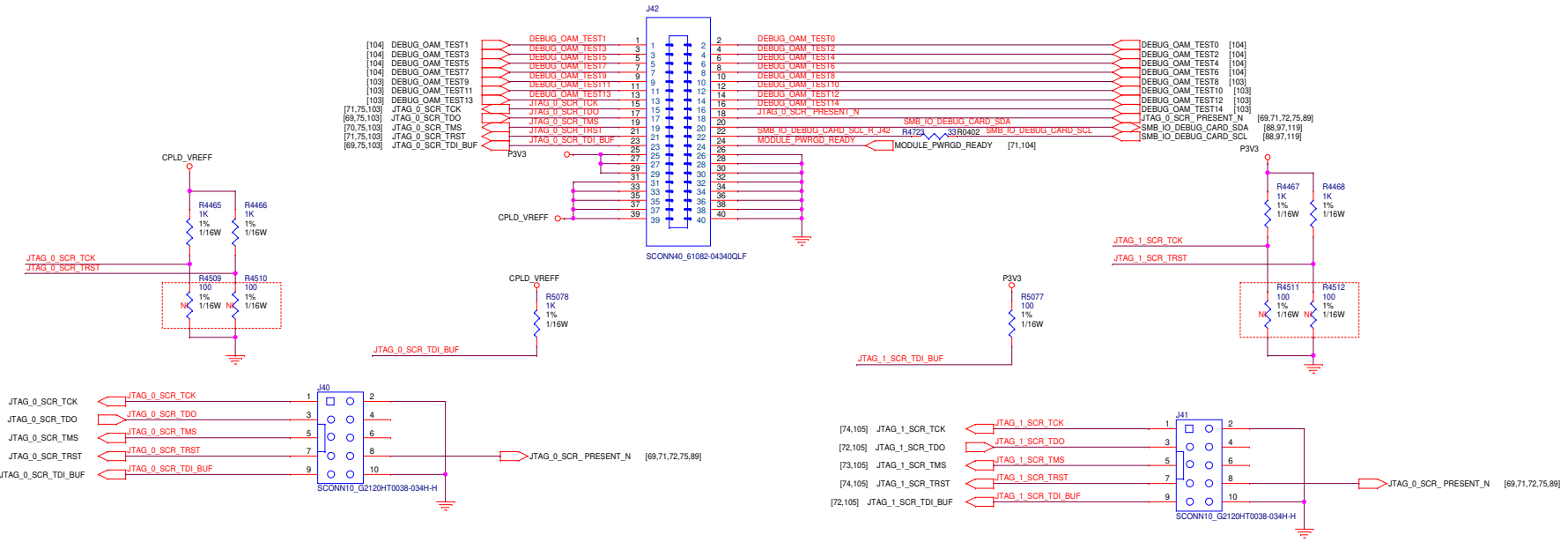
JTAG1 (2/3)

Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 73 of 155



JTAG1 (3/3)

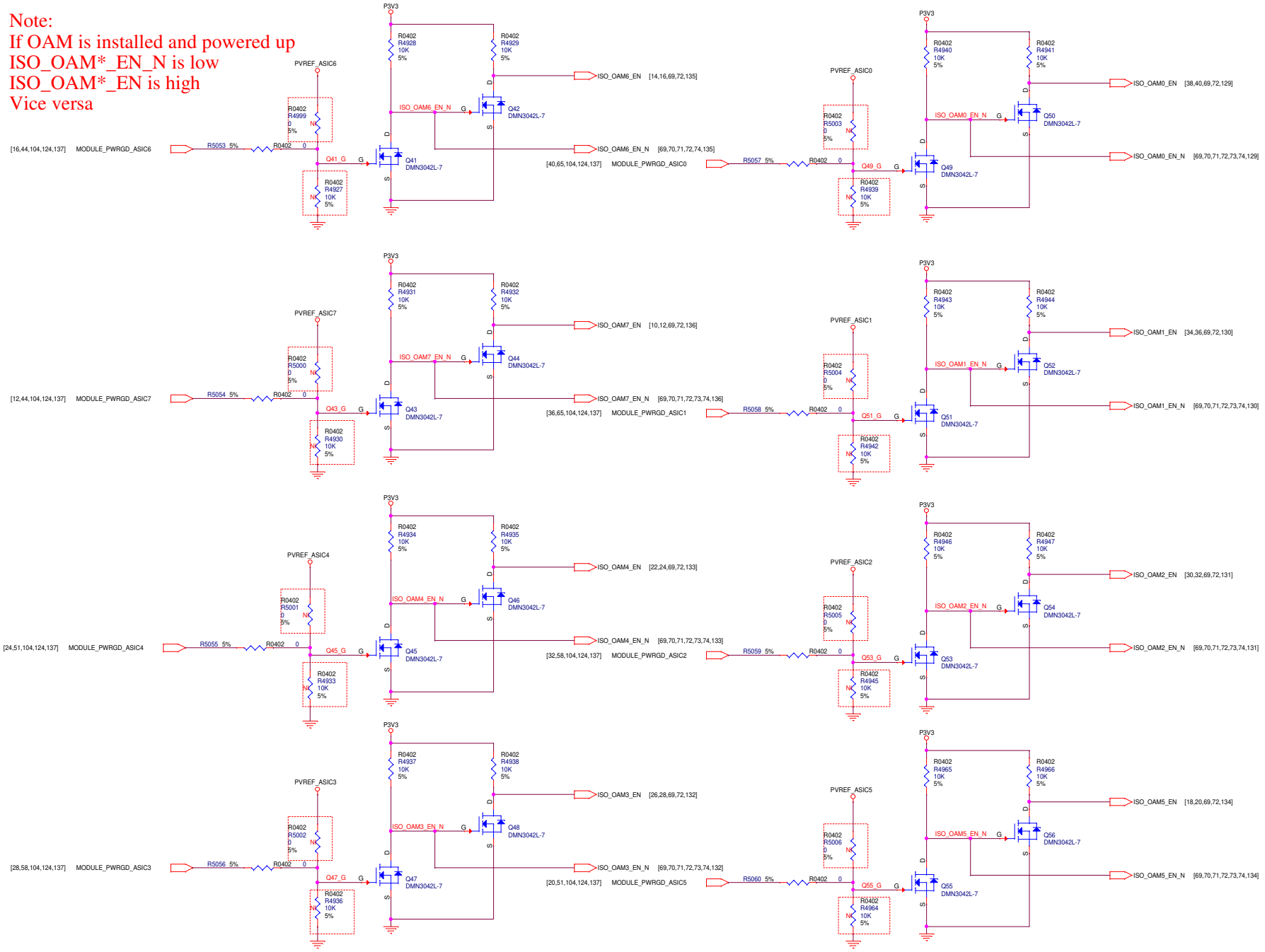
Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP BASEBOARD OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 74 of 155



MODULE_DEBUG_CONN

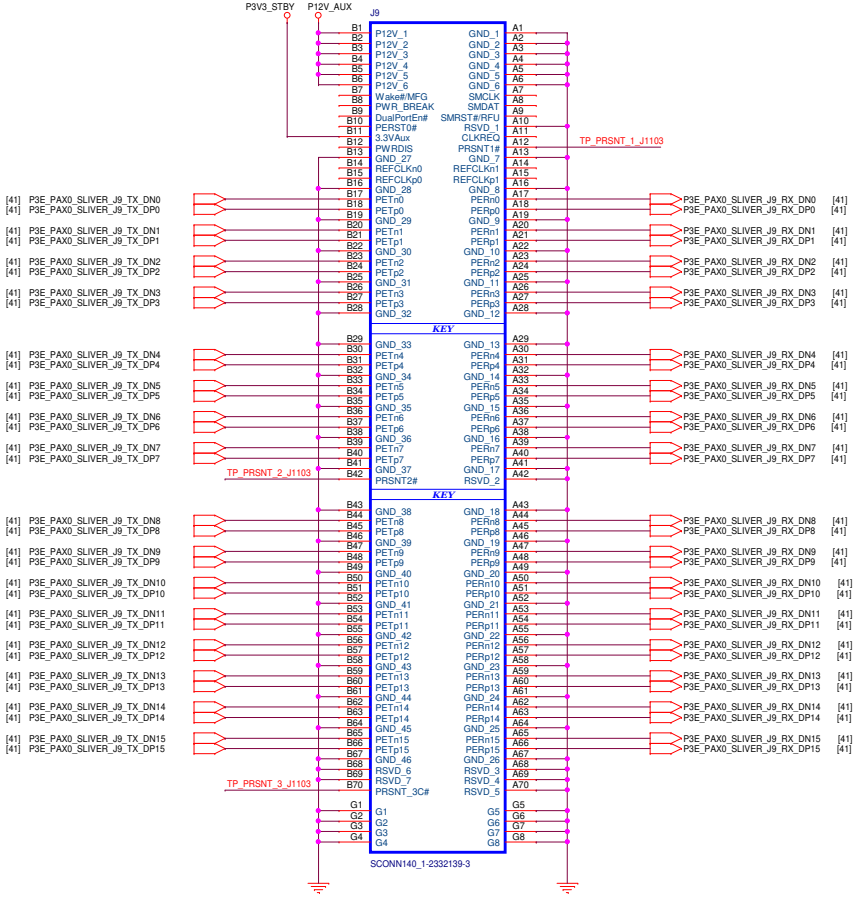
Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 75 of 155

Note:
If OAM is installed and powered up
ISO_OAM*_EN_N is low
ISO_OAM*_EN is high
Vice versa



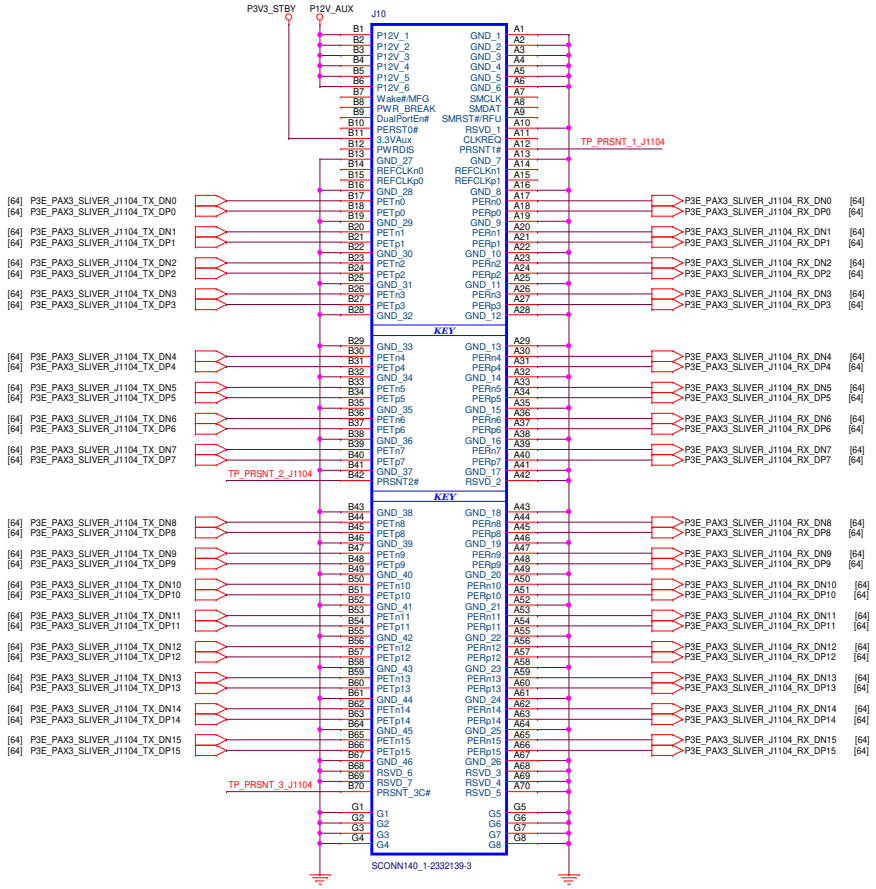
ISOLATOIN CONTROL

Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 76 of 155



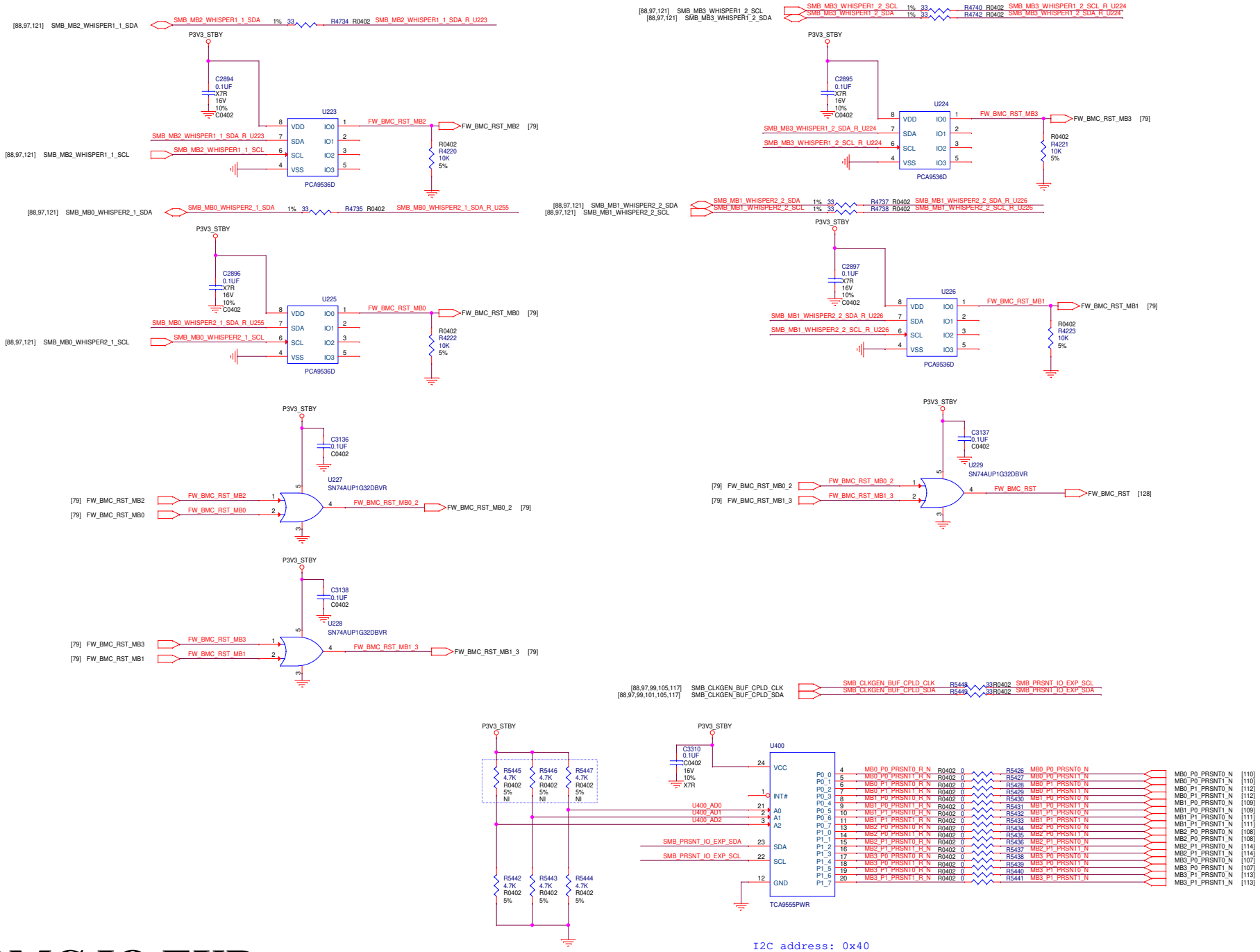
SLIVER CONN (1/2)

Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 77 of 155



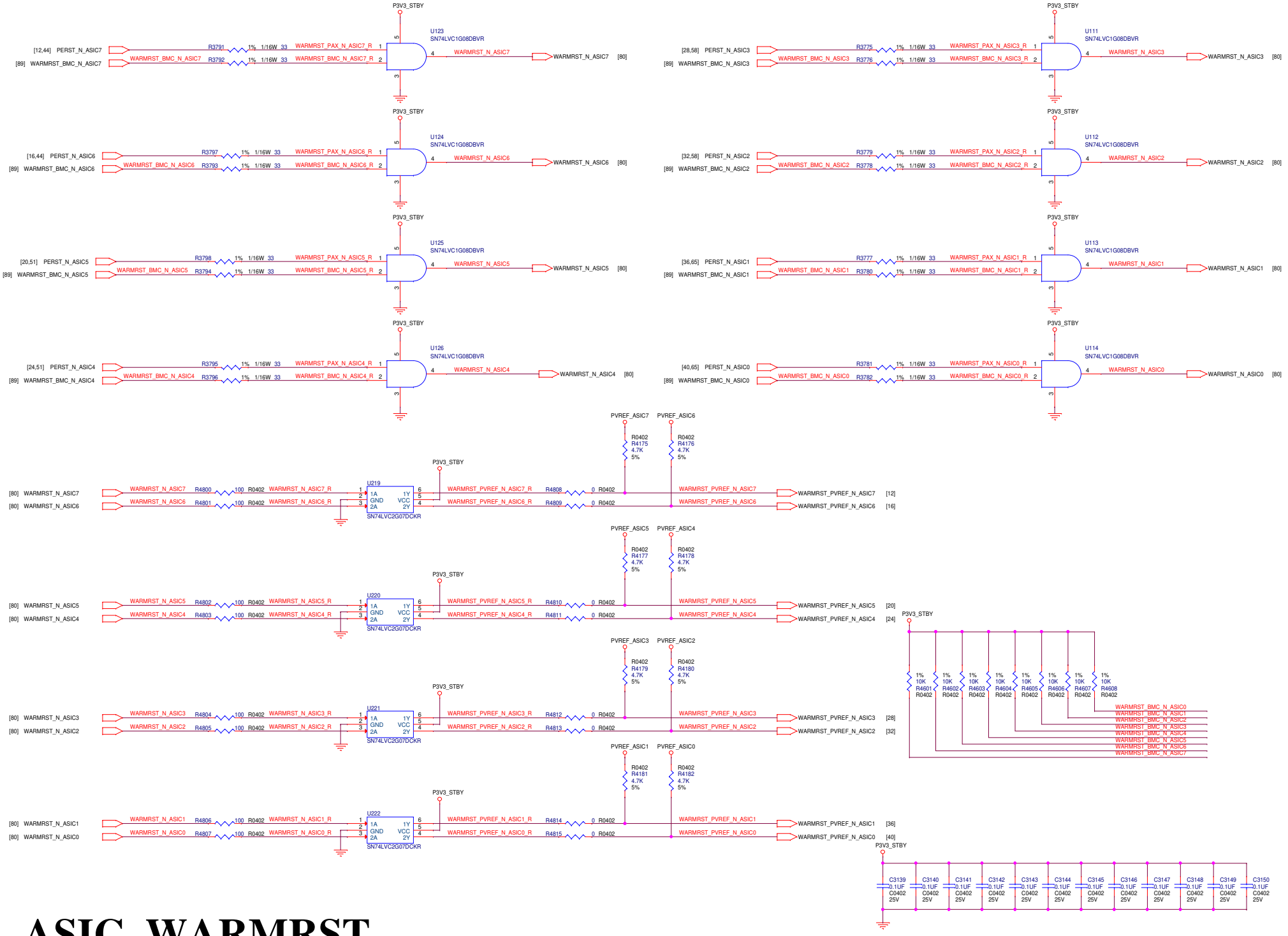
SLIVER CONN (2/2)

Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 78 of 155



BMC IO EXP

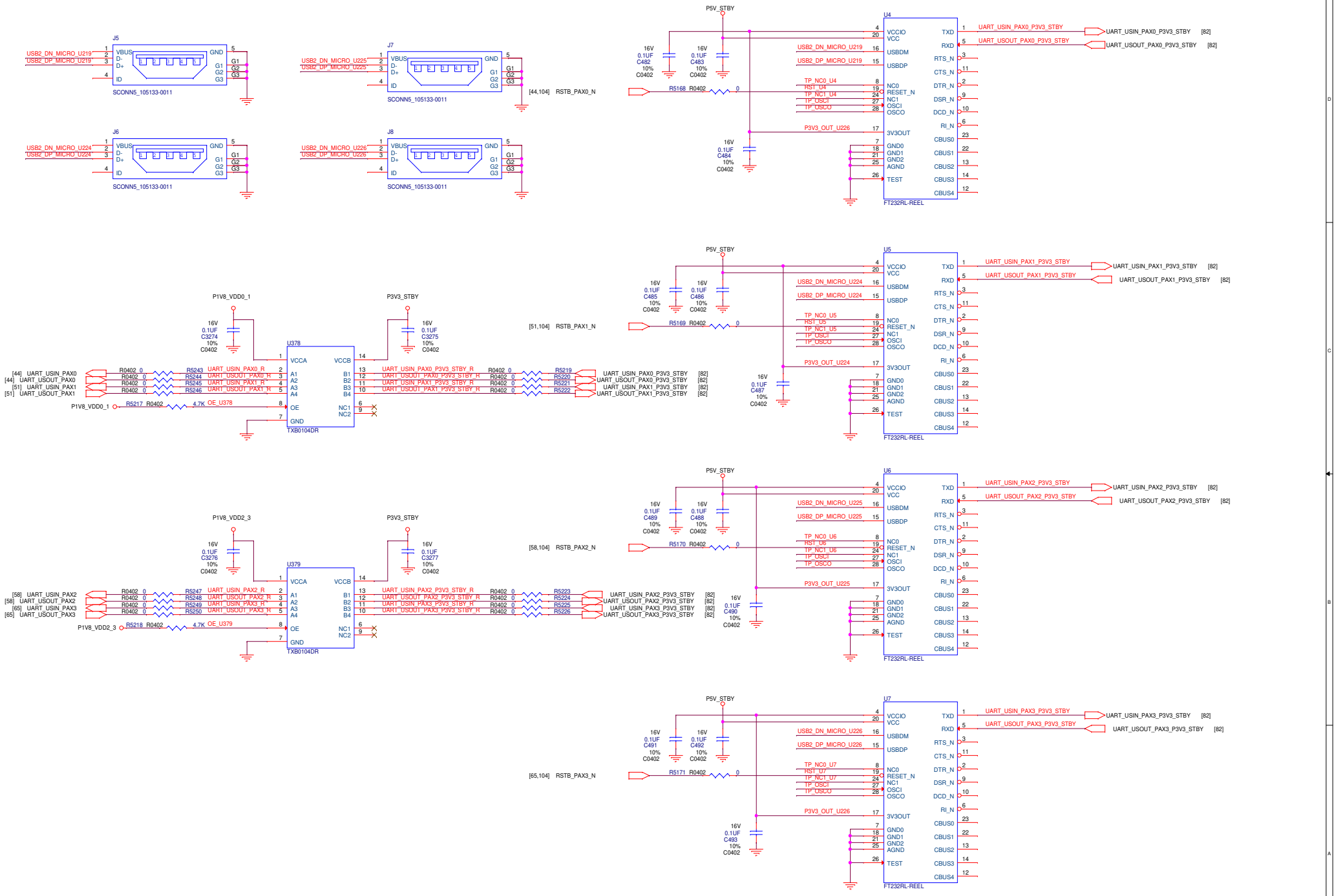
Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022
				Page Title Cover Page
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ASIC_WARMRST

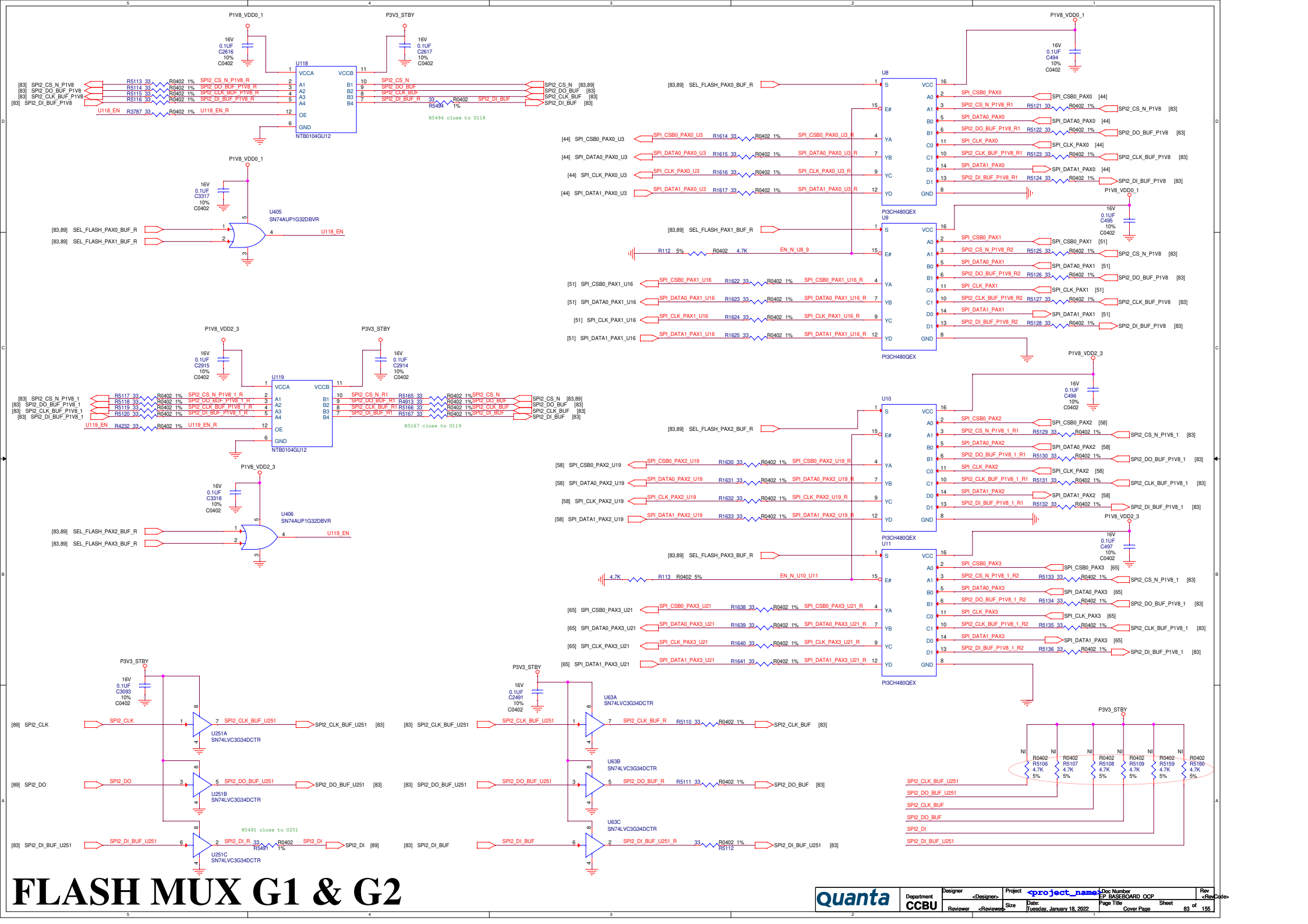
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		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 80 of 155

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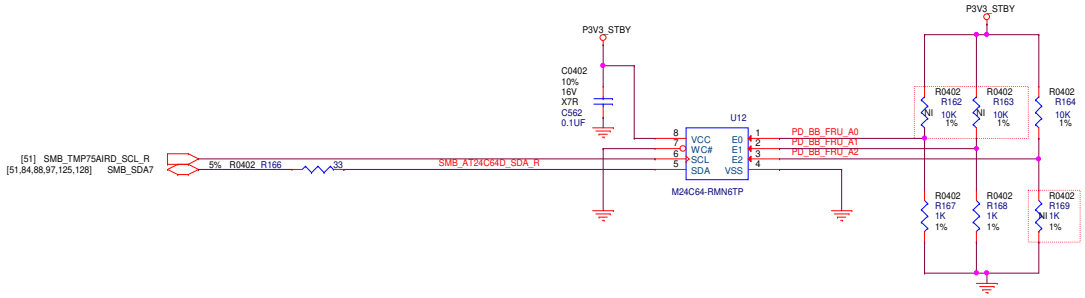
UART TO USB

Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 82 of 155

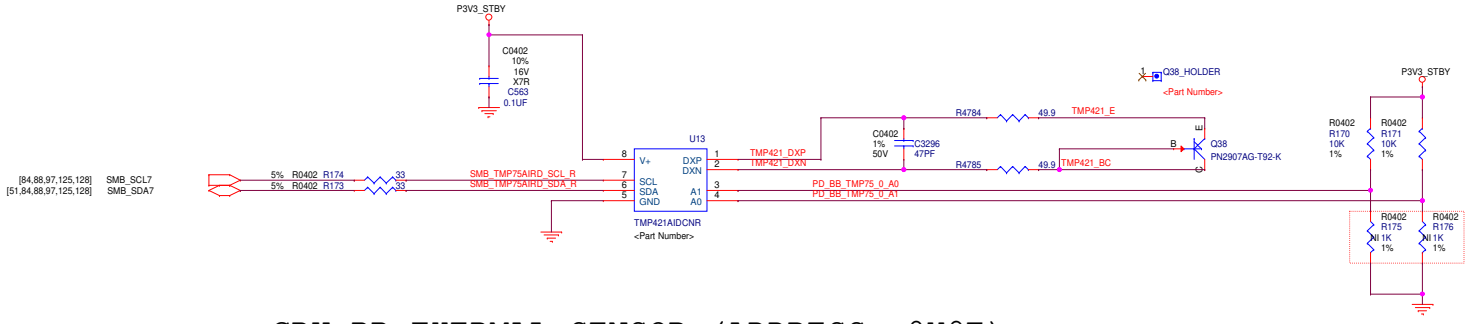


FLASH MUX G1 & G2

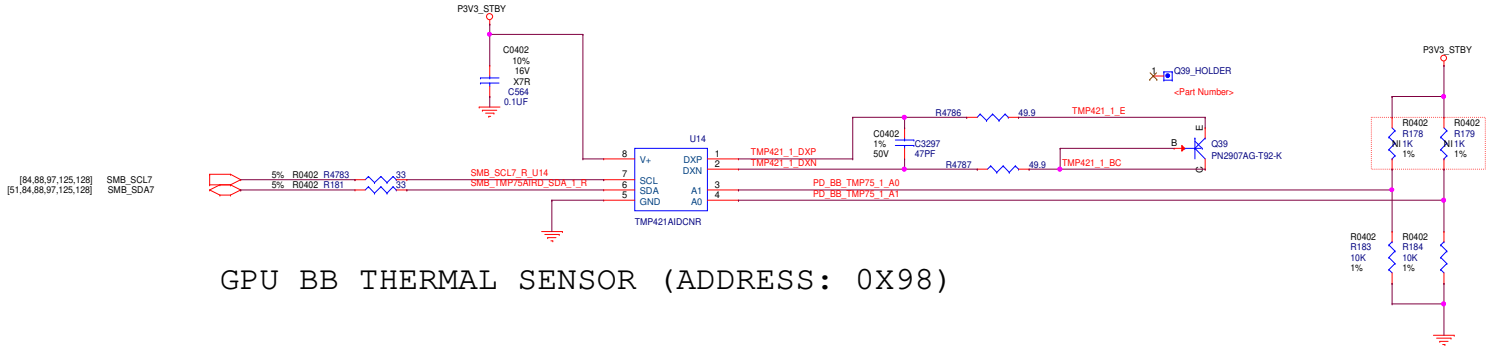
Quanta	Department: CCBU	Designer: <Designer>	Project: <project_name>
		Reviewer: <Reviewer>	Size
		Date: Tuesday, January 18, 2022	Doc Number: EP_BASEBOARD_OCP
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BB FRU (SMB9 ADDRESS: 0XA8)



GPU BB THERMAL SENSOR (ADDRESS: 0X9E)



GPU BB THERMAL SENSOR (ADDRESS: 0X98)

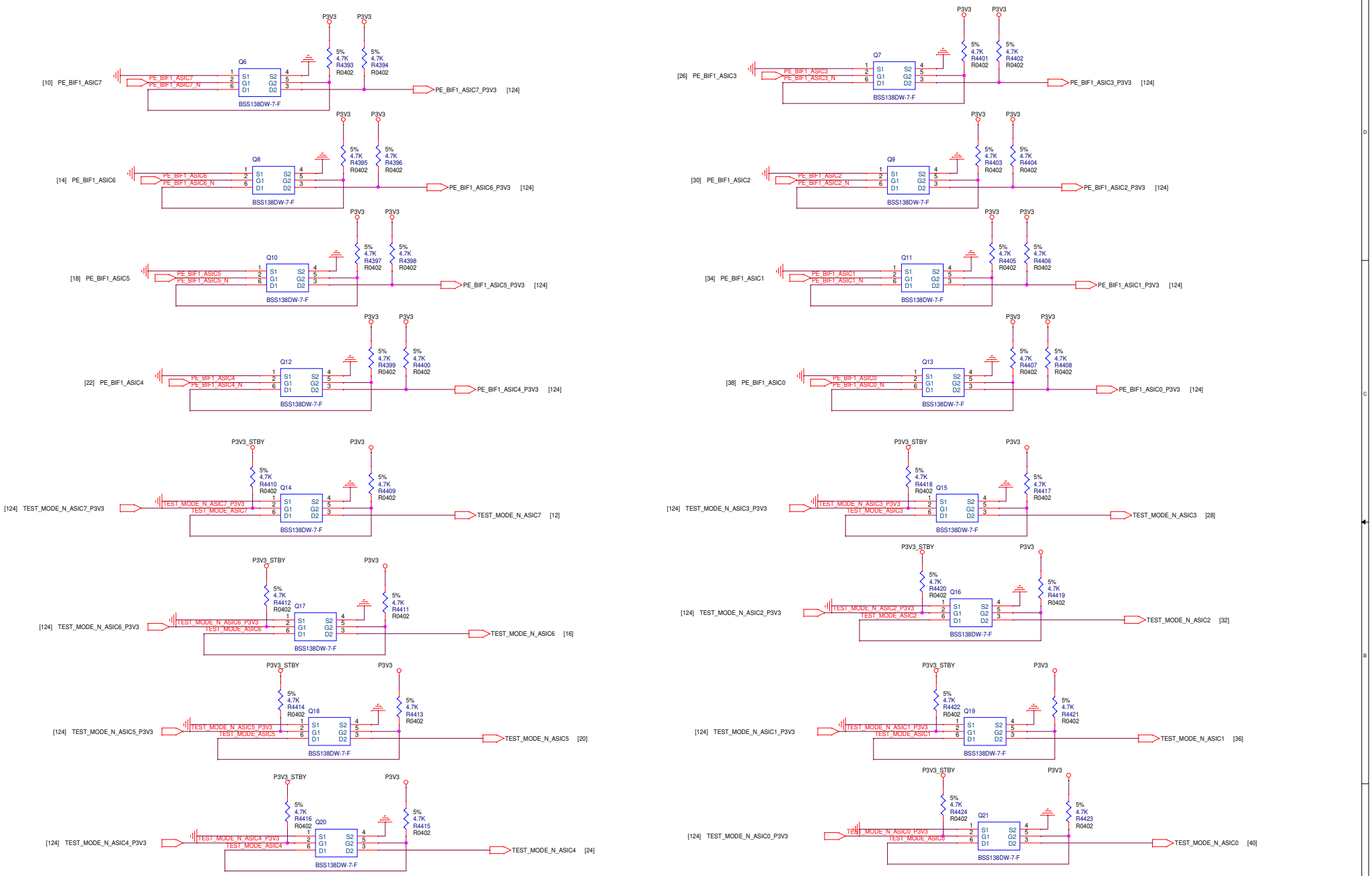
GPU_NODE1_FRU_TEMP_SENSOR

Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 84 of 155

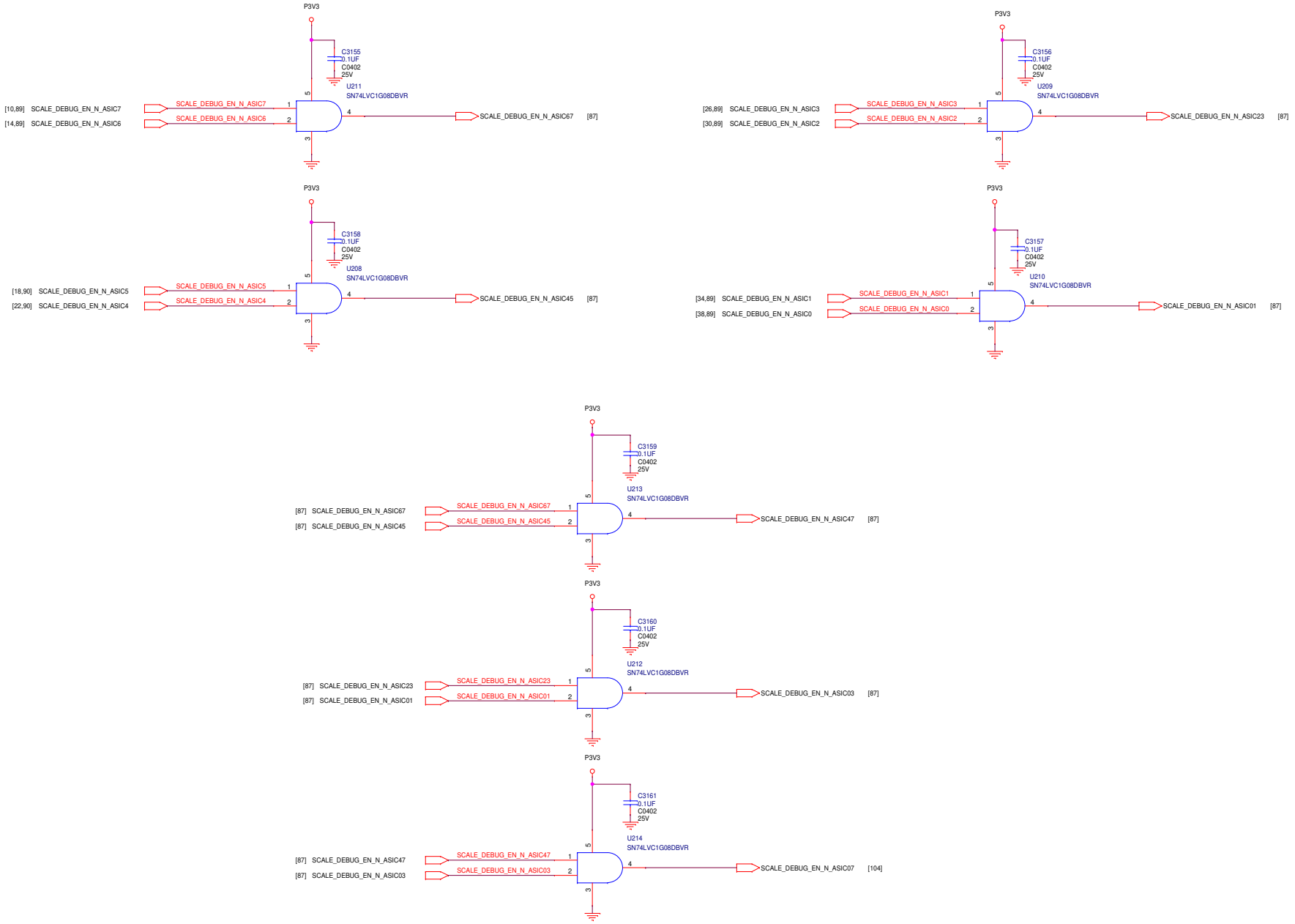


LEVEL SHIFT

Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 85 of 155

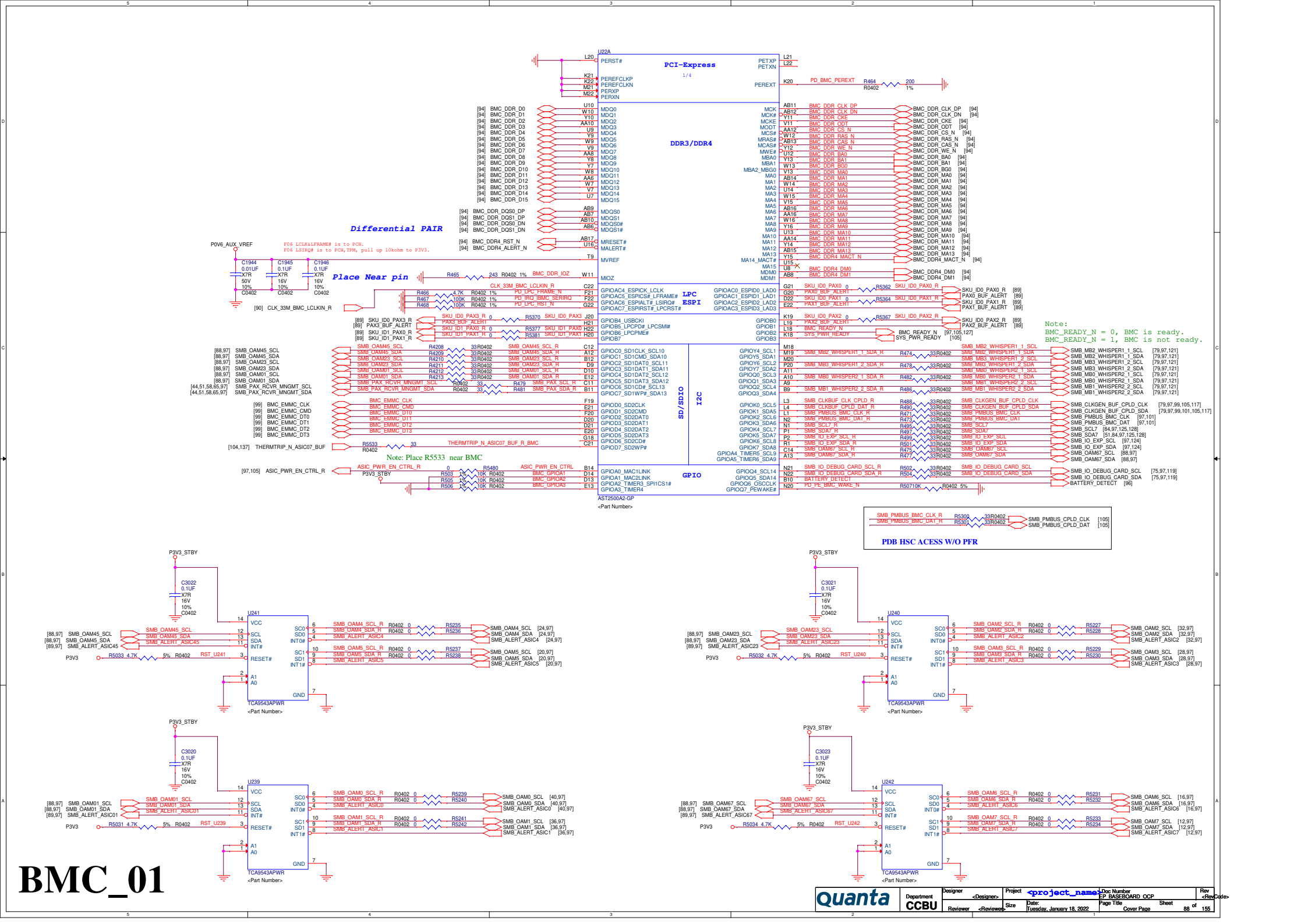


Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 86 of 155



SCALE_DEBUG

Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
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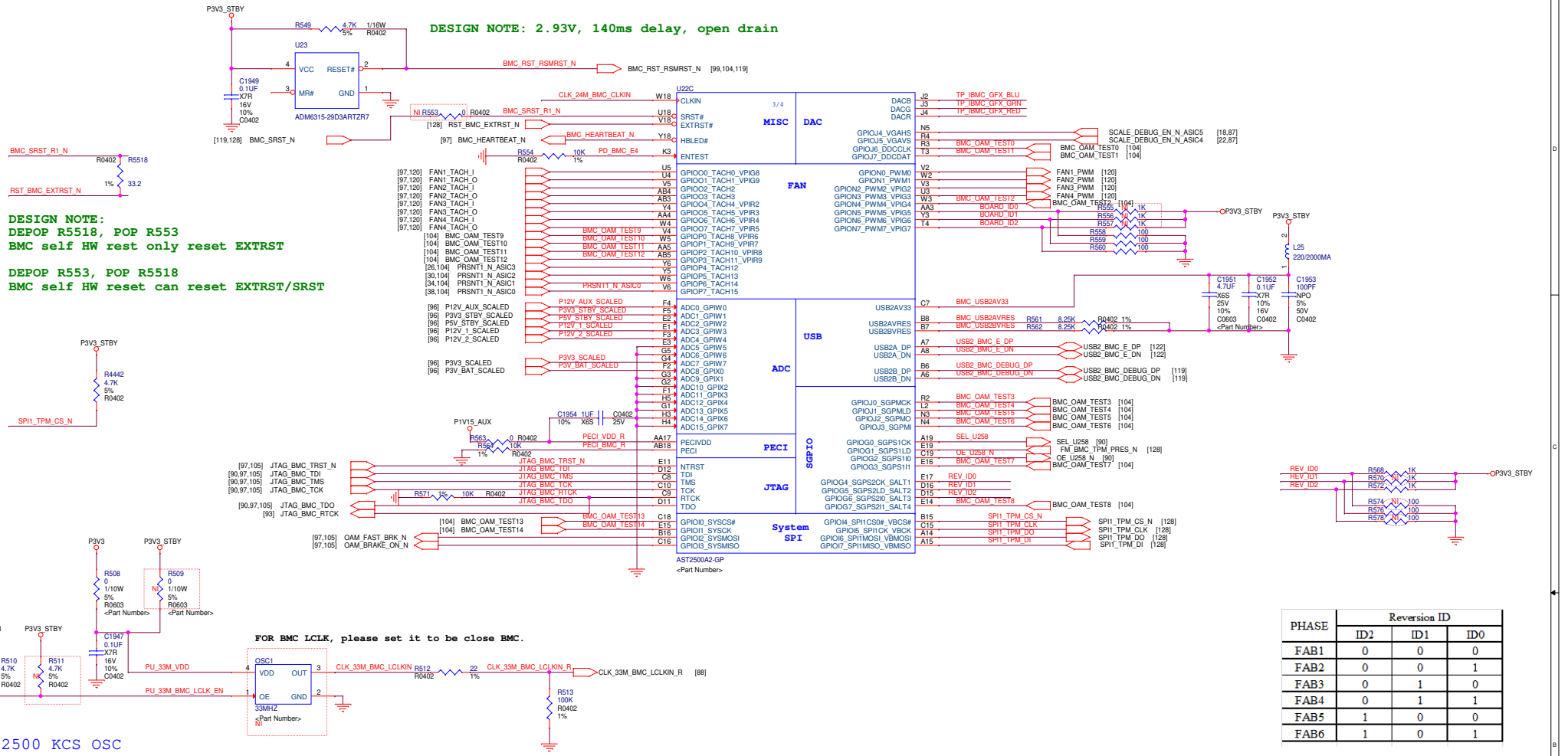

PCI-Express
1/4
DDR3/DDR4
Differential PAIR
Place Near pin
LPC
ESPI
SD/SDIO
I2C
GPIO
AST2500A2-GP
<Part Number>
F06 LCLK&LFRAME# is to PCH.
F06 LSIRQ# is to PCH,IPM, pull up 10kohm to P3V3.
Note: Place R5533 near BMC
Note:
BMC_READY_N = 0, BMC is ready.
BMC_READY_N = 1, BMC is not ready.
PDB HSC ACESS W/O PFR
U241
U240
U239
U242
TCA9543APWR
P3V3_STBY
BMC_01
Quanta
Department
CCBU
Designer
<Designer>
Reviewer
<Reviewer>
Project
<project_name>
Size
Date:
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	PCIe SW config pin		
PAX config	ID0_PAX*	ID1_PAX*	SKU_ID0_PAX*
8S+8A PAX0	0	0	0
8S+8A PAX1	0	1	0
8S+8A PAX2	1	0	0
8S+8A PAX3	1	1	0
2S+8A PAX0	0	0	1
2S+8A PAX1	0	1	1
2S+8A PAX2	1	0	1
2S+8A PAX3	1	1	1

Note: SKU_ID1_PAX* is RSVD function

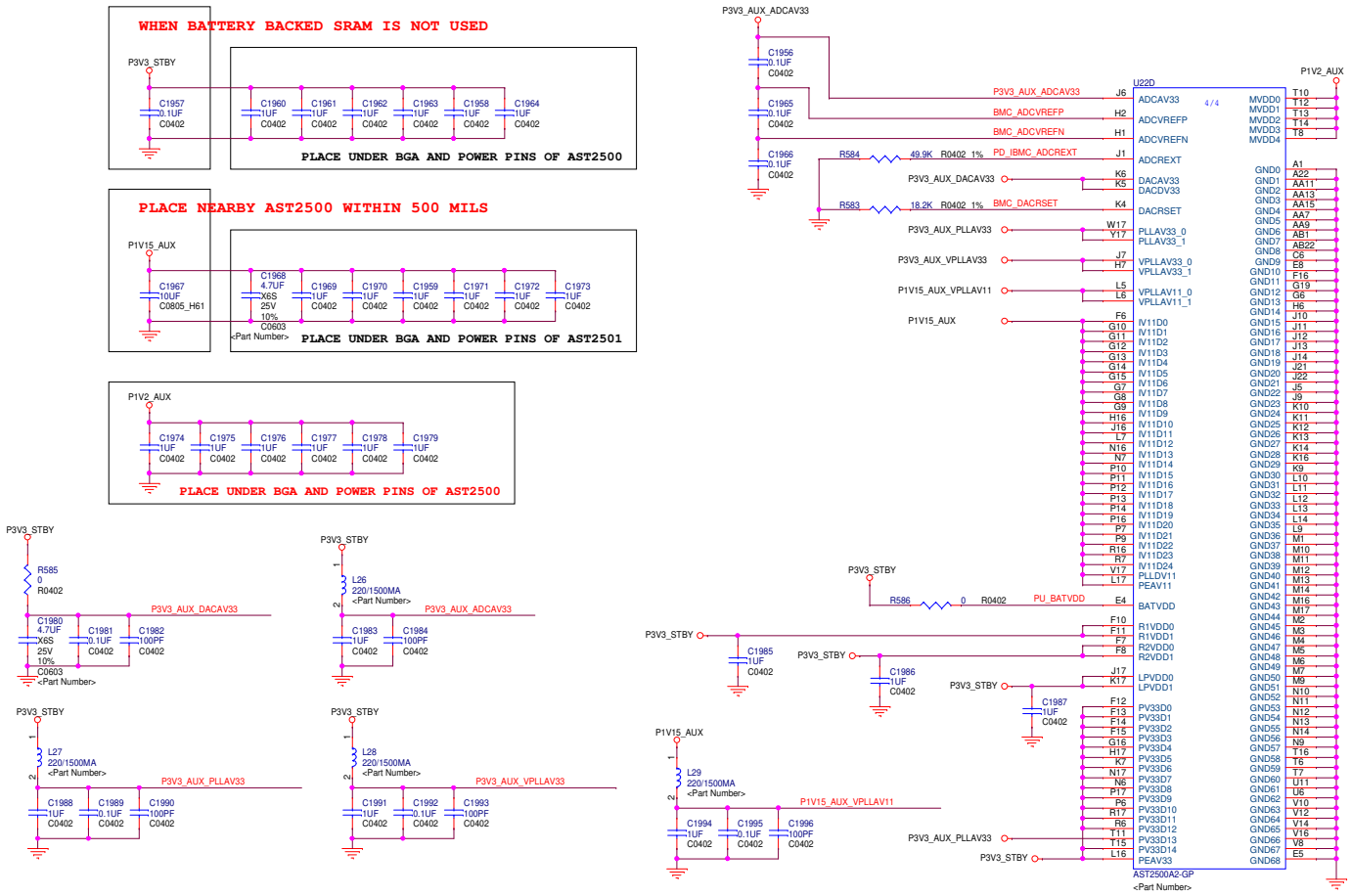
Quanta | Department: CCBU | Designer: <Designer> | Reviewer: <Reviewer> | Project: <project_name> | Size | Date: Tuesday, January 18, 2022 | Doc Number: EP BASEBOARD OCP | Rev: <RevCode> | Page Title: Cover Page | Sheet 89 of 155



PHASE	Reversion ID		
	ID2	ID1	ID0
FAB1	0	0	0
FAB2	0	0	1
FAB3	0	1	0
FAB4	0	1	1
FAB5	1	0	0
FAB6	1	0	1

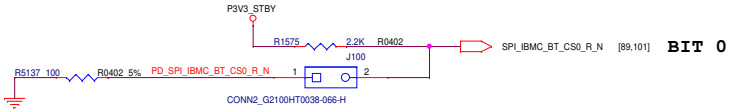
BMC_03

Quanta	Department: CCBU	Designer: <Designer>	Project: <project_name>	Doc Number: EP_BASEBOARD_OCP	Rev: <RevCode>
		Reviewer: <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title: Cover Page — Sheet 90 of 155



BMC_04

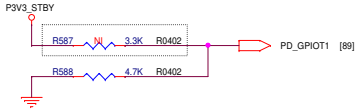
Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 91 of 155



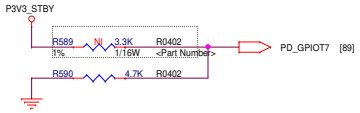
BIT 0

GPIO strap pins definition.

Pin	Definition	Value = 0	Value = 1	Valid for PN
GPIOS4	VGA memory size selection	16 MB	64 MB	2500/2530
GPIOS5	Reserved	**Default**	*Disallowed*	2500/2530
GPIOS6	Enable VGA BIOS ROM	No	Yes	2500/2530
GPIOS7	VGA Class Code selection	Non-VGA	VGA	2500/2530
GPIOZ4	Enable BMC 2nd boot watchdog timer	No	Yes	2500/2520/2530
GPIOZ5	Select USBCKI input frequency	24MHz	48MHz	2500/2520/2530
GPIOZ6	Disable LPC to decode SuperIO address	No	Yes	2500/2520/2530
GPIOZ7	Enable fast reset mode	No	**Yes**	2500/2520/2530

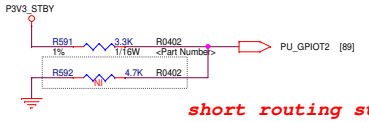


BIT 6



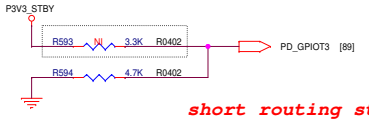
BIT 7

short routing stub



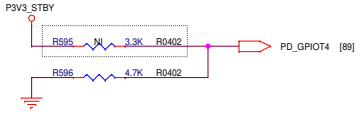
BIT 12

short routing stub



BIT 13

short routing stub



BIT 16

```
BIT 0 (DEDICATED STRAP PIN)
BALL NAME: FWSPICS0#
*0=ENABLE BMC
1=DISABLE BMC

BIT 1 (NOT IN HW STRAP)
RESERVED

BIT 2 (OPTIONAL STRAP PIN)
VGA MEMORY SIZE SELECTION

BIT 3 (OPTIONAL STRAP PIN)
IT ONLY BE USED FOR GPIO FUNCTION DUE TO BIT30 IS DISABLED
BALL NAME: GPIOS4

BIT 4 (OPTIONAL STRAP PIN)
IT ONLY BE USED FOR GPIO FUNCTION DUE TO BIT30 IS DISABLED
BALL NAME: GPIOS5

BIT 5 (OPTIONAL STRAP PIN)
IT ONLY BE USED FOR GPIO FUNCTION DUE TO BIT30 IS DISABLED
BALL NAME: GPIOS6
0=NO VGA BIOS ROM,VGA BIOS IS MERGED IN THE SYSTEM BIOS
1=ENABLE DEDICATED VGA BIOS ROM

BIT 6 (DEDICATEDL STRAP PIN)
BALL NAME: RGMII1TXCTL
*0=RMII/NCSI
1=RGMII

BIT 7 (DEDICATEDL STRAP PIN)
BALL NAME: RGMII2TXCTL
0=RMII/NCSI
*1=RGMII

BIT 8 (NOT IN HW STRAP)
CPU/AXI CLOCK FREQUENCY RATIO SELECTION
0=SELECT CPU/AXI= 1:1
1=SELECT CPU/AXI= 2:1

BIT 11:9 (NOT IN HW STRAP)
AXI/AHB CLOCK FREQUENCY RATIO SELECTION
000=UNDEFINED
001=SELECT AXI:AHB= 2:1
010=SELECT AXI:AHB= 3:1
011=SELECT AXI:AHB= 4:1
100=SELECT AXI:AHB= 5:1
101=SELECT AXI:AHB= 6:1
110=SELECT AXI:AHB= 7:1
111=SELECT AXI:AHB= 8:1

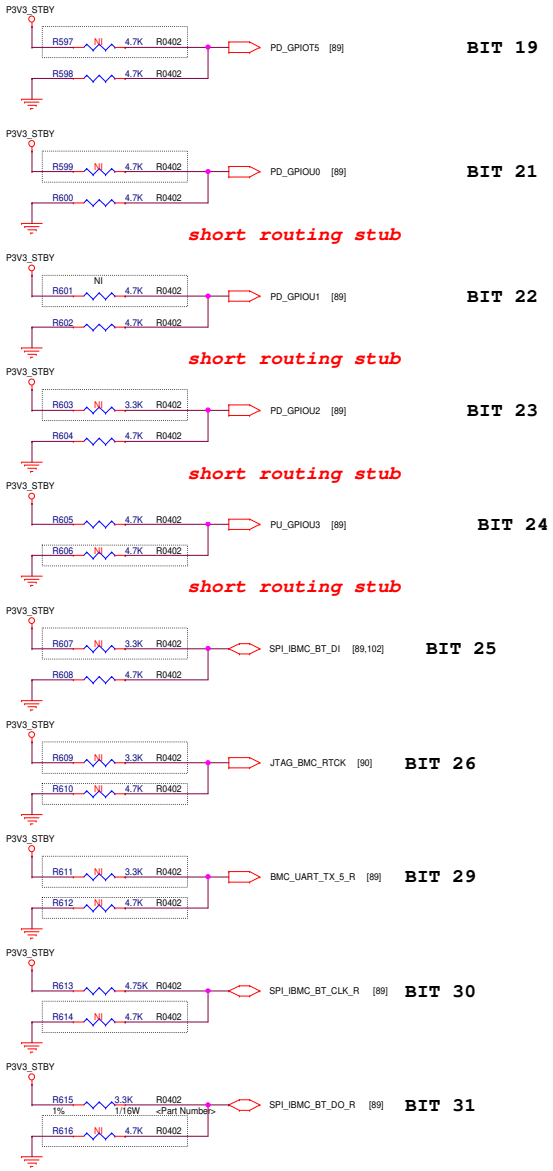
BIT 12 (DEDICATEDL STRAP PIN)
BALL NAME: RGMII1TXD0
BIT 13 (DEDICATEDL STRAP PIN)
BALL NAME: GPIOT3
*00=DISABLE SPI INTERFACE
01=ENABLE SPI MASTER
10=ENABLE SPI MASTER AND SPI SLAVE TO AHB BRIDGE
11=ENABLE SPI PASS-THROUGH

BIT 14 (NOT IN HW STRAP)
SELECT DEDICATED LPC RESET INPUT
0=LPC RESET IS SHARED WITH PCIE RESET PIN
1=LPC RESET IS LOCATED AT PIN NUMBER G22,SHARED WITH GPIOAC7

BIT 15 (OPTIONAL STRAP PIN)
IT ONLY BE USED FOR GPIO FUNCTION DUE TO BIT30 IS DISABLED
BALL NAME: GPIOS7
0=SELECT THE CLASS CODE FOR VIDEO DEVICE
1=SELECT THE CLASS CODE FOR VGA DEVICE

BIT 16 (DEDICATED STRAP PIN)
BALL NAME: GPIOT4
*0=DECODE 0X2E
1=DECODE 0X4E
```

BMC_HW_STRAPPING_1




```
BIT 17 (OPTIONAL STRAP PIN)
IT ONLY BE USED FOR GPIO FUNCTION DUE TO BIT30 IS DISABLED
BALL NAME: GPIOZ4
0=DISABLE
1=ENABLE BMC 2ND BOOT WATCHDOGTIMER START COUNTING AT POWER UP.

BIT 18 (OPTIONAL STRAP PIN)
IT ONLY BE USED FOR GPIO FUNCTION DUE TO BIT30 IS DISABLED
BALL NAME: GPIOZ5
0=24MHz
1=48MHz

BIT 19 (DEDICATED STRAP PIN)
BALL NAME: GPIOT5
*0=DISABLE ACPI
1=ENABLE ACPI

BIT 20 (OPTIONAL STRAP PIN)
IT ONLY BE USED FOR GPIO FUNCTION DUE TO BIT30 IS DISABLED
BALL NAME: GPIOZ6
0=ENABLE ADDRESS DECODING
1=DISABLE ADDRESS DECODING

BIT 21 (DEDICATED STRAP PIN)
BALL NAME: RGMII2TXD0
*0=DISABLE PASS THROUGH CAN BE ENABLED BY SCU8C[11:8]
1=ENABLE PASS-THROUGH AT POWER ON.
    GPIOD0 -> GPIOD1
    GPIOD2 -> GPIOD3
    GPIOD4 -> GPIOD5
    GPIOD6 -> GPIOD7

BIT 22 (DEDICATED STRAP PIN)
BALL NAME: RGMII2TXD1
*0=DISABLE PASS THROUGH CAN BE ENABLED BY SCU8C[15:12]
1=ENABLE PASS-THROUGH AT POWER ON.
    GPIOE0 -> GPIOE1
    GPIOE2 -> GPIOE3
    GPIOE4 -> GPIOE5
    GPIOE6 -> GPIOE7

BIT 23 (DEDICATED STRAP PIN)
BALL NAME: RGMII2TXD2
*0=CLKIN IS 24 MHZ AND USBCKI NOT USED
1=CLKIN IS 25 MHZ AND USBCKI= 24/48 MHZ (DETERMINED BY BIT[18])

BIT 24 (DEDICATED STRAP PIN)
BALL NAME: RGMII2TXD3
0=DDR3 SDRAM
*1=DDR4 SDRAM

BIT 25 (DEDICATED STRAP PIN)
BALL NAME: FWSPIMISO
0=LPC MODE (ONLY FOR PSPO STAGE)
1=ESPI MODE (NORMAL STAGE)

BIT 26 (DEDICATED STRAP PIN)
BALL NAME: RTCK
0=ESPI RESPOND W/O FLASH ATTACHED
1=ESPI RESPOND W/ FLASH ATTACHED

BIT 27 (OPTIONAL STRAP PIN)
IT ONLY BE USED FOR GPIO FUNCTION DUE TO BIT30 IS DISABLED
BALL NAME: GPIOZ7
0=LONG RESET MODE, NORMAL OPERATION
1=FAST RESET MODE, FOR ICE DEBUGGER CONNECTION

BIT 28 (NOT IN HW STRAP)
RESERVED

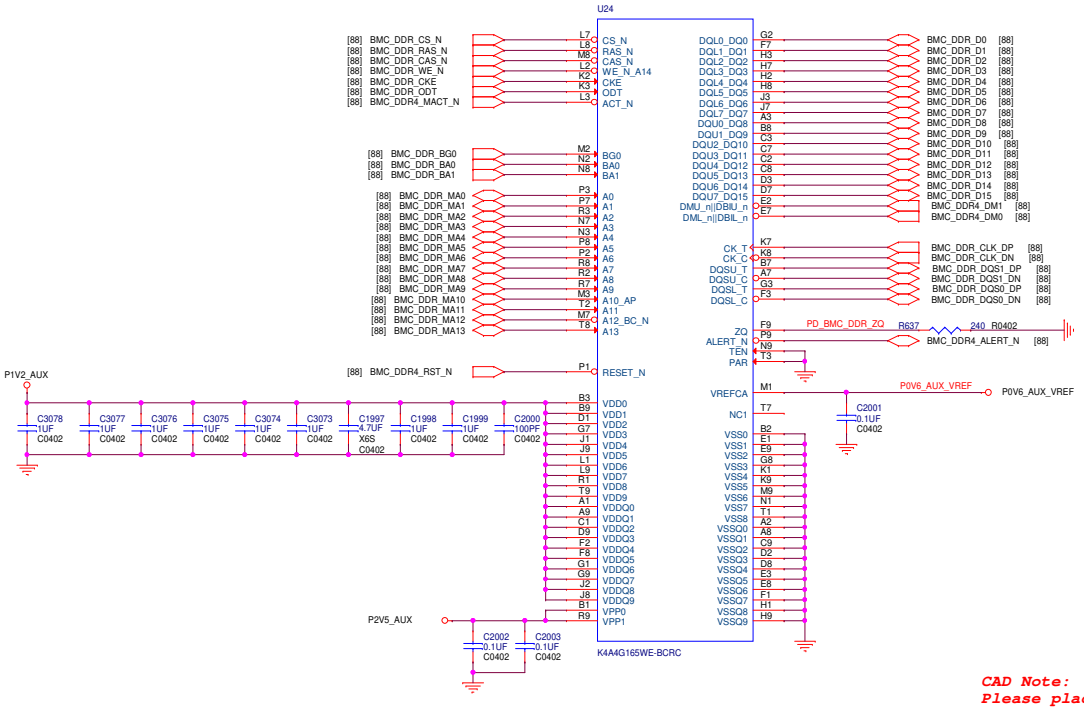
BIT 29 (DEDICATED STRAP PIN)
BALL NAME: TXD5
0=SELECT UART1 AS BMC CONSOLE PORT
1=SELECT UART5 AS BMC CONSOLE PORT

BIT 30 (DEDICATED STRAP PIN)
BALL NAME: FWSPICK
0=DISABLE
1=ENABLE

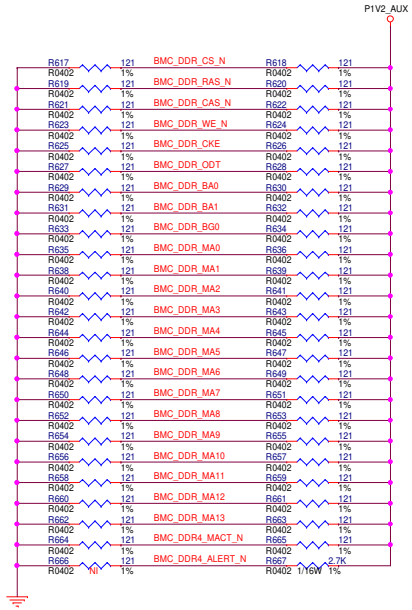
BIT 31 (DEDICATED STRAP PIN)
BALL NAME: FWSPIMOSI
0=DISABLE
*1=ENABLE
```

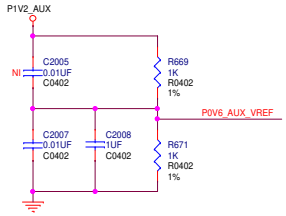
BMC_HW_STRAPPING_2

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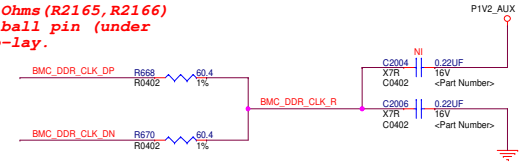
Termination





TRACE WIDTH >= 15 MILS

CAD Note:
Please placement 60 Ohms(R2165,R2166) close to DDR memory ball pin (under board pin) and do co-lay.

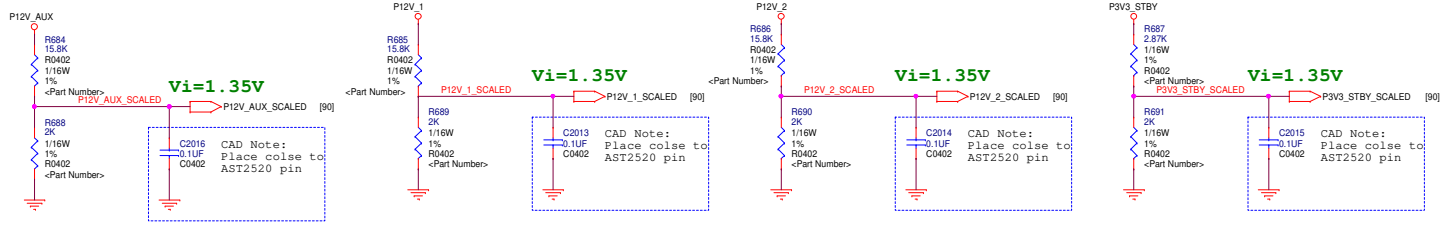


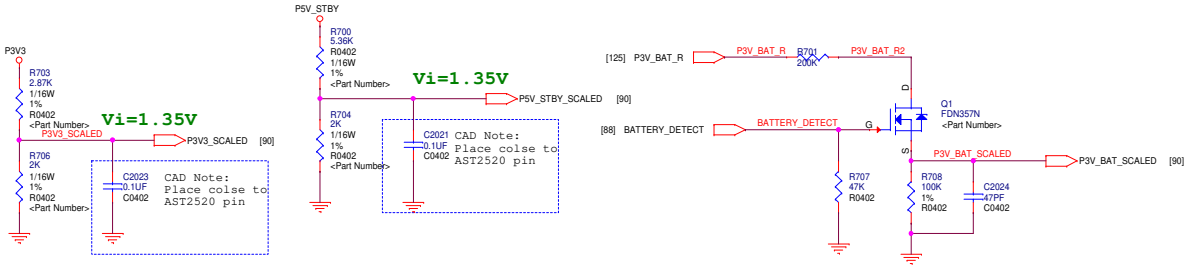
CAD Note:
C1461,C1462 need placement close to 60 Ohms and do co-lay.

BMC_DDRIII_IV_SDRAM

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ROUTE ALL ADC NETS AT 6 MILLS WIDE

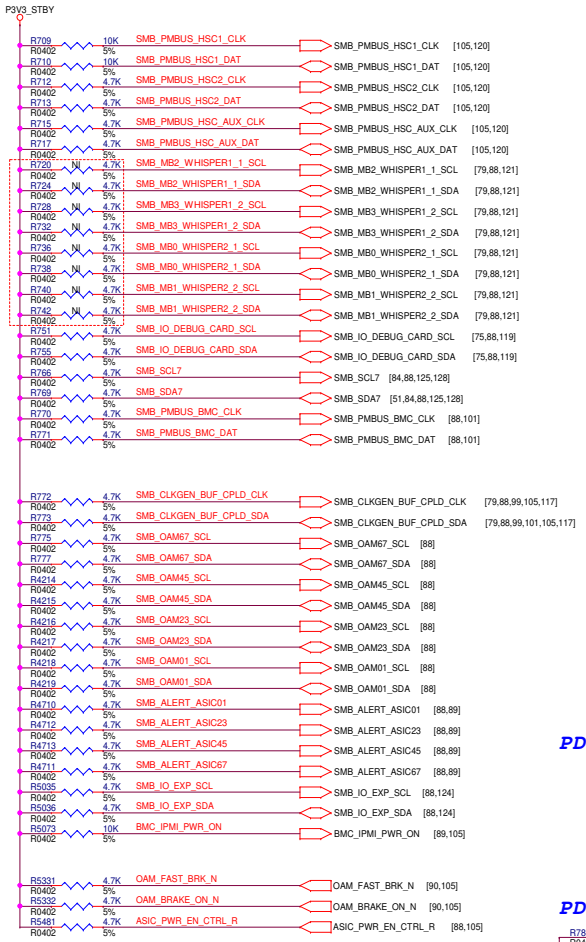




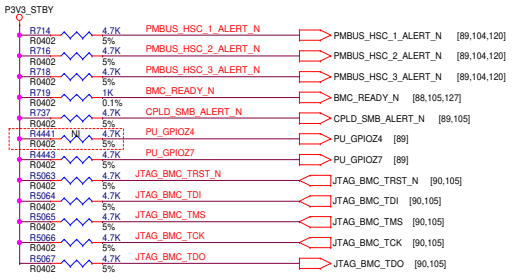
BMC VOLTAGE SENSOR

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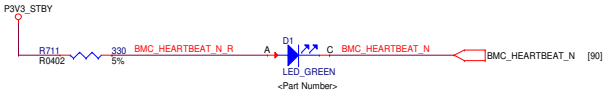
PU OF BMC SMBUS

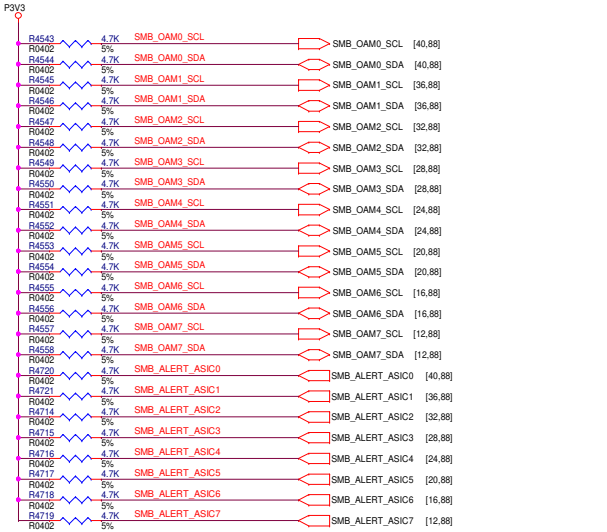


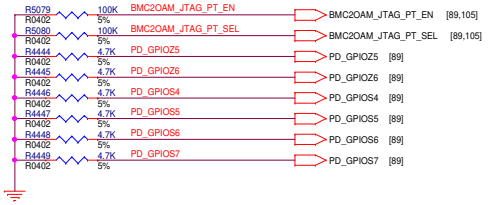
PU OF SIDE BAND



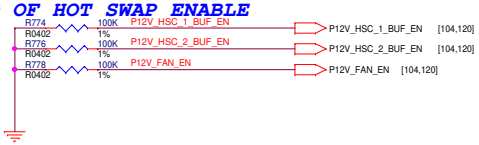
HEART BEATING LED



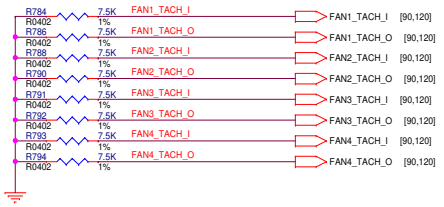


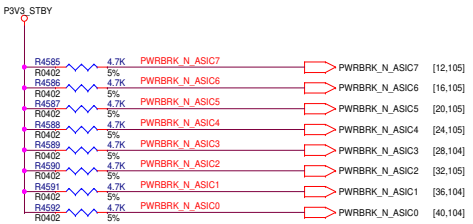


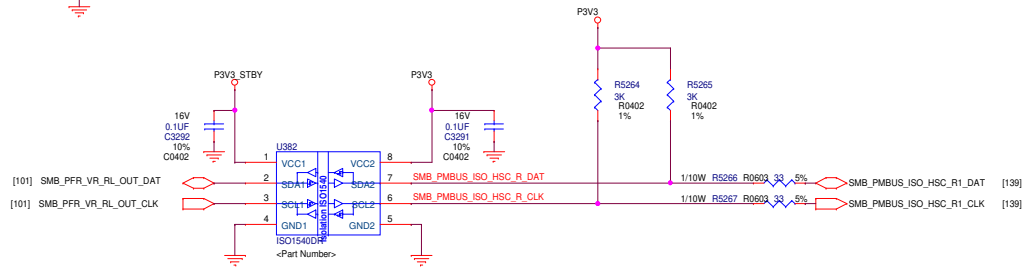
PD OF HOT SWAP ENABLE



PD OF FAN TACH



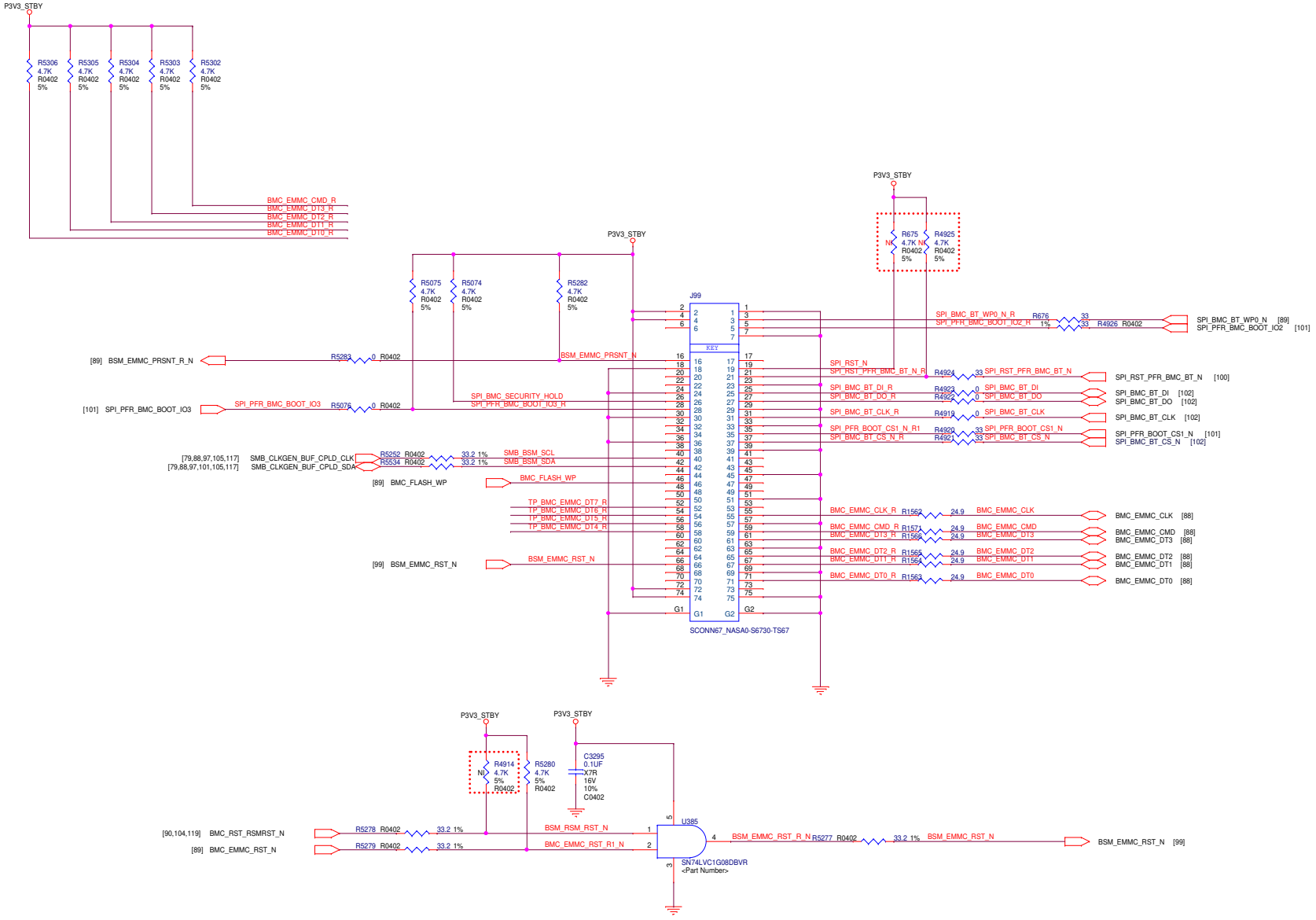




BMC&CPLD PULL UP

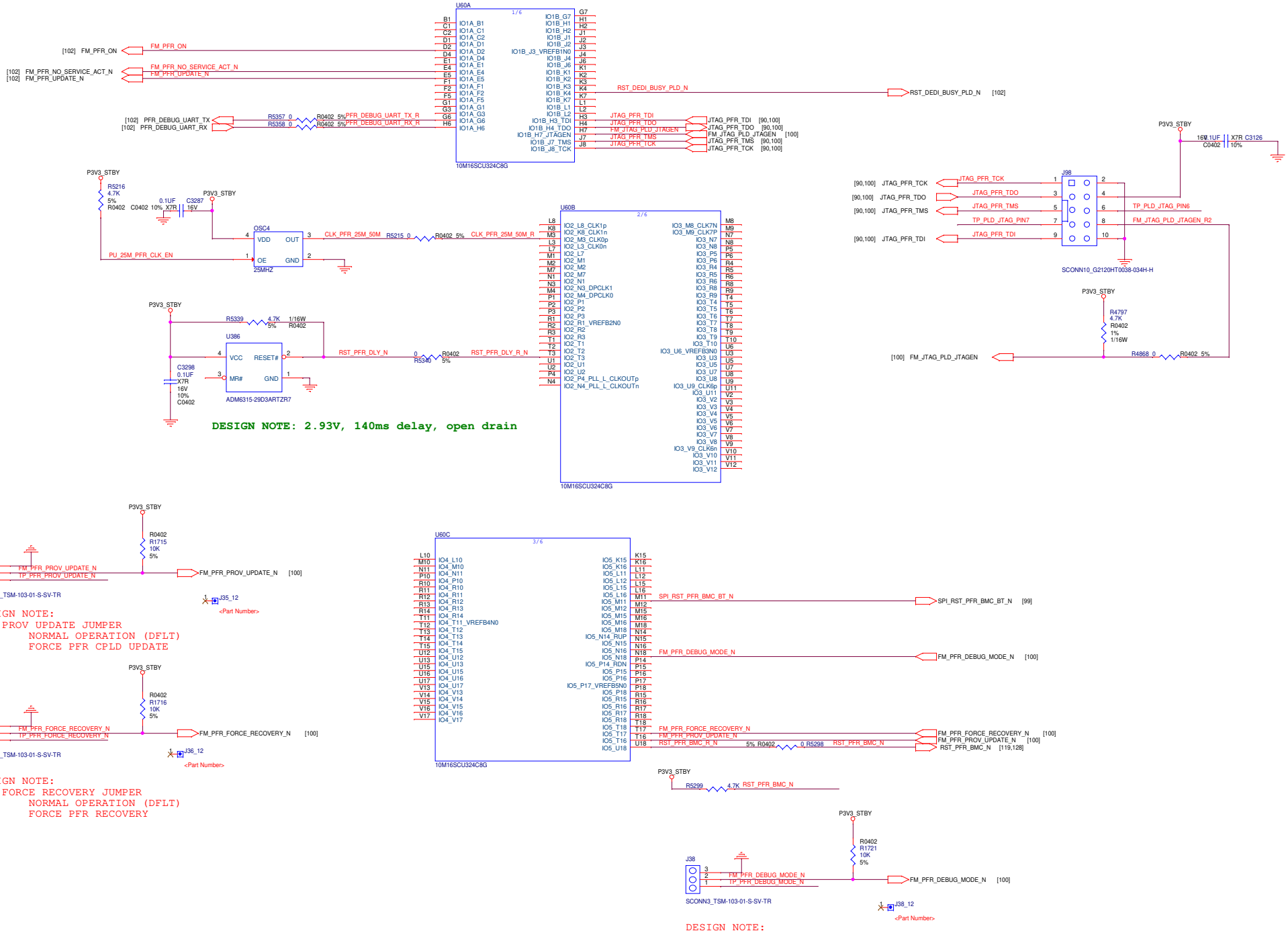
Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
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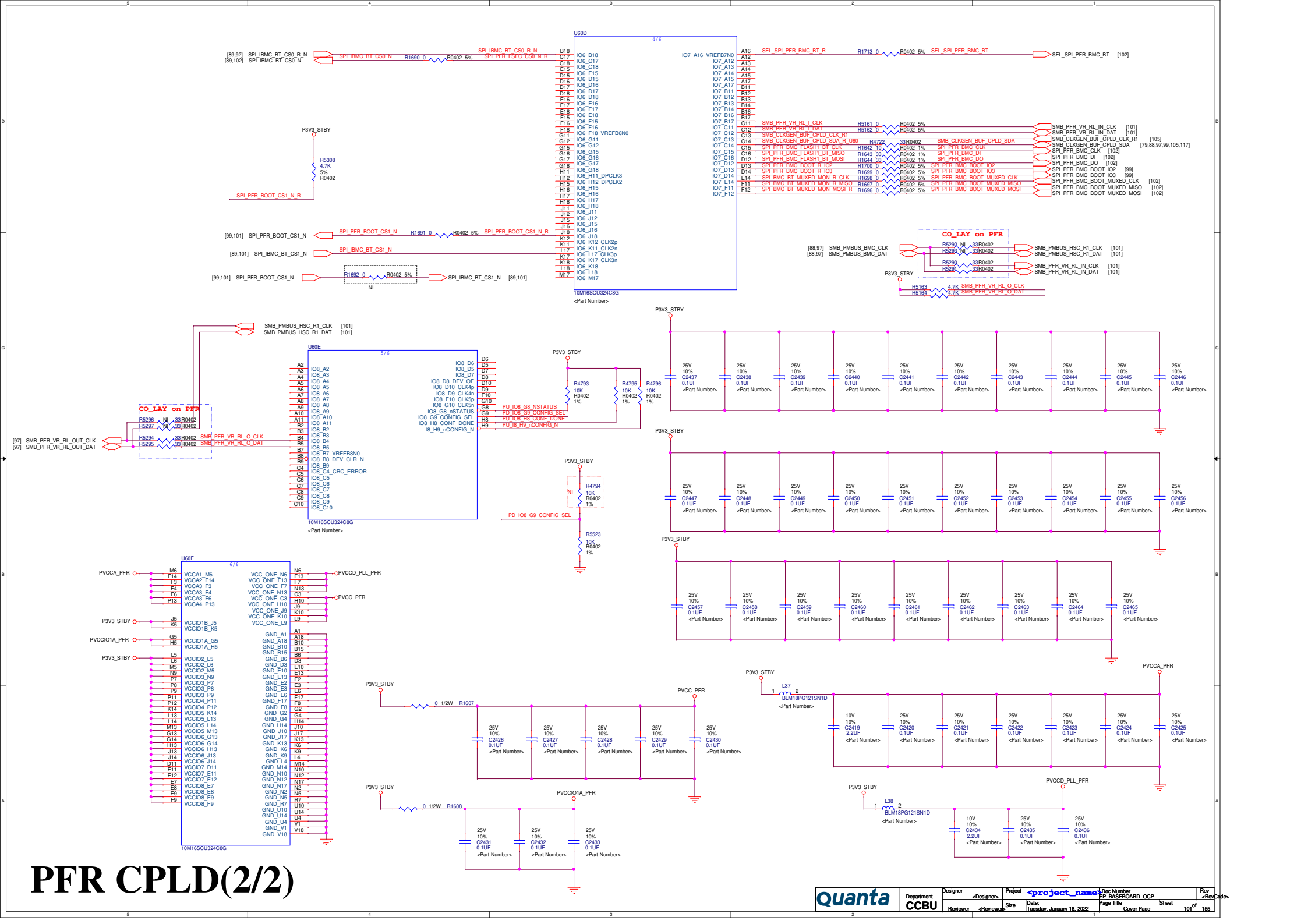
M.2 CONNECTOR

Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 99 of 155

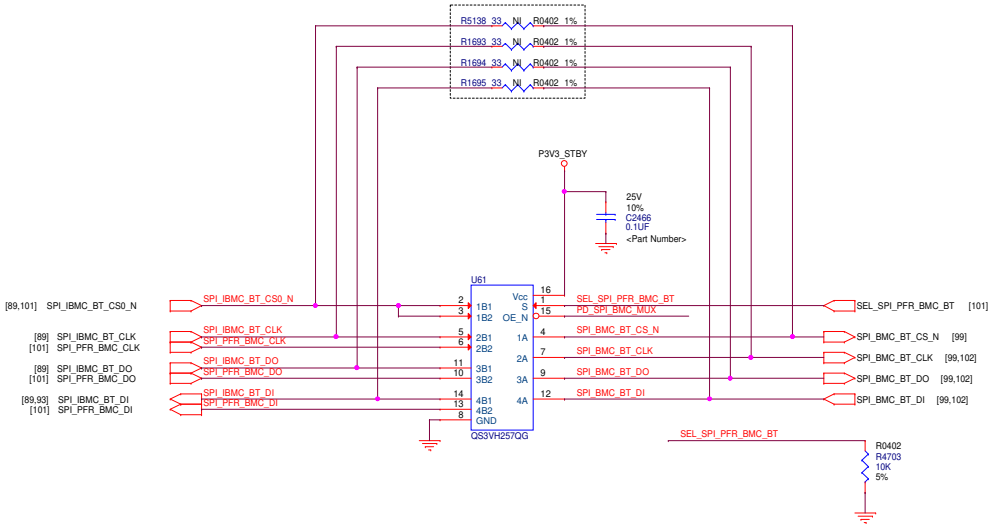


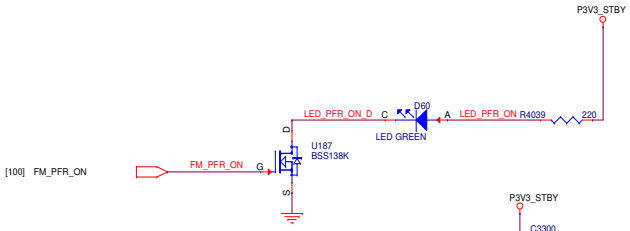
PFR CPLD(1/2)

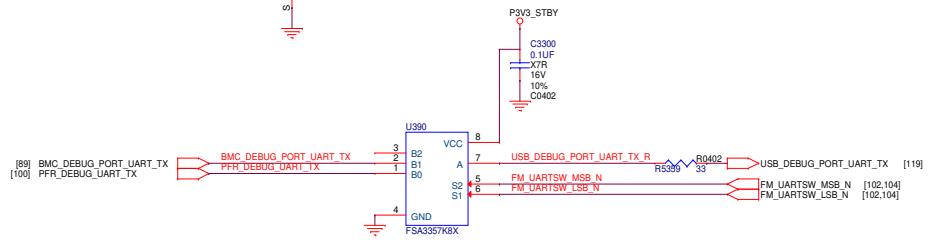
Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP BASEBOARD OCP	Rev <RevCode>
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U60D
4/6
10M16SCU324C8G
<Part Number>
SPI_IBMC_BT_CS0_N_R
SPI_PFR_FSEC_CS0_N_R
SPI_IBMC_BT_CS0_N
R1690 0
R0402 5%
SPI_PFR_BOOT_CS1_N_R
SPI_PFR_BOOT_CS1_N
R1691 0
SPI_IBMC_BT_CS1_N
R1692 0
NI
P3V3_STBY
R5308
4.7K
5%
R0402
SEL_SPI_PFR_BMC_BT_R
R1713 0
SEL_SPI_PFR_BMC_BT
SMB_PFR_VR_RL_I_CLK
SMB_PFR_VR_RL_I_DAT
SMB_CLKGEN_BUF_CPLD_CLK_R1
SMB_CLKGEN_BUF_CPLD_SDA_R_U60
R4722
33R0402
SMB_CLKGEN_BUF_CPLD_SDA
SPI_PFR_BMC_FLASH1_BT_CLK
SPI_PFR_BMC_FLASH1_BT_MISO
SPI_PFR_BMC_FLASH1_BT_MOSI
SPI_PFR_BMC_BOOT_R_IO2
SPI_PFR_BMC_BOOT_R_IO3
SPI_BMC_BT_MUXED_MON_R_CLK
SPI_BMC_BT_MUXED_MON_R_MISO
SPI_BMC_BT_MUXED_MON_MOSI_R
CO_LAY on PFR
SMB_PMBUS_BMC_CLK
SMB_PMBUS_BMC_DAT
SMB_PMBUS_HSC_R1_CLK
SMB_PMBUS_HSC_R1_DAT
SMB_PFR_VR_RL_IN_CLK
SMB_PFR_VR_RL_IN_DAT
SMB_PFR_VR_RL_O_CLK
SMB_PFR_VR_RL_O_DAT
R5163 4.7K
R5164 4.7K
U60E
5/6
SMB_PMBUS_HSC_R1_CLK [101]
SMB_PMBUS_HSC_R1_DAT [101]
SMB_PFR_VR_RL_OUT_CLK [97]
SMB_PFR_VR_RL_OUT_DAT [97]
R5296 NI 33R0402
R5297 NI 33R0402
R5294 33R0402
R5295 33R0402
SMB_PFR_VR_RL_O_CLK
SMB_PFR_VR_RL_O_DAT
PU_IO8_G8_NSTATUS
PD_IO8_G9_CONFIG_SEL
PU_IO8_H8_CONF_DONE
PU_I8_H9_nCONFIG_N
R4793 10K R0402 1%
R4795 10K R0402 1%
R4796 10K R0402 1%
R4794 NI 10K R0402 1%
R5523 10K R0402 1%
U60F
6/6
10M16SCU324C8G
PVCCA_PFR
PVCCIO1A_PFR
PVCCD_PLL_PFR
PVCC_PFR
R1607 0 1/2W
R1608 0 1/2W
L37 BLM18PG121SN1D
L38 BLM18PG121SN1D
C2419 2.2UF
C2434 2.2UF
25V 10% 0.1UF
10V 10%
<Part Number>
Quanta
Department CCBU
Designer <Designer>
Reviewer <Reviewer>
Project <project_name>
Size
Date: Tuesday, January 18, 2022
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Rev <RevCode>
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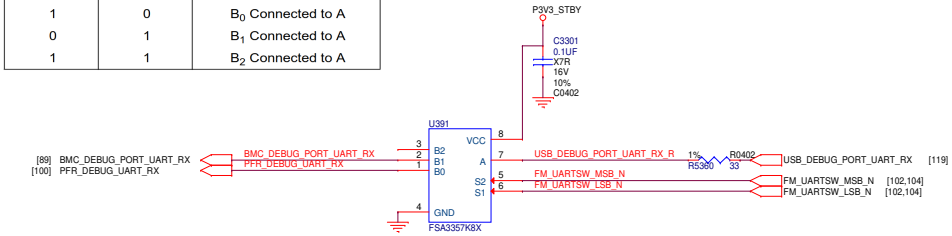
PFR CPLD(2/2)

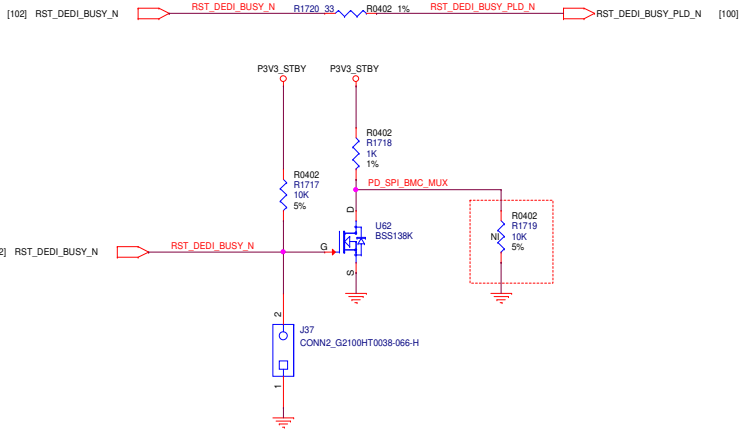


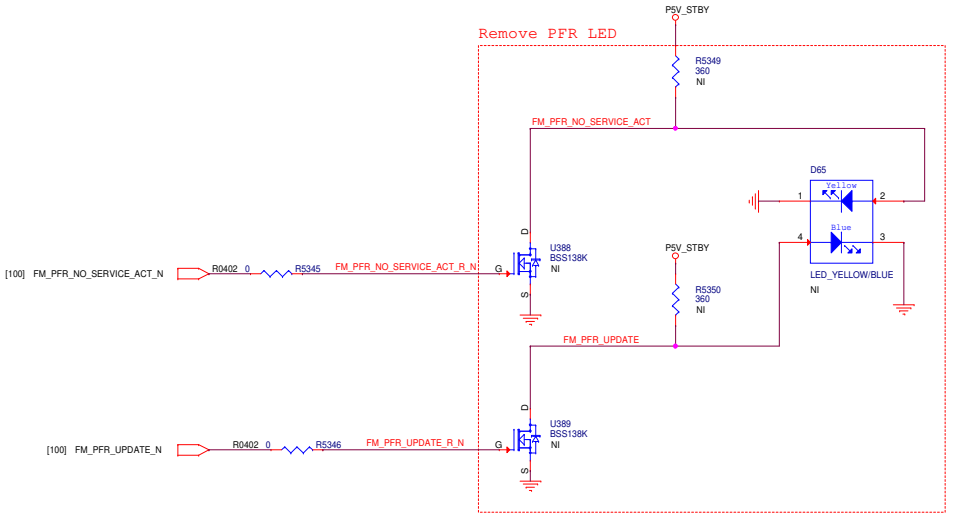




S_1	S_2	Function
0	0	No Connection
1	0	B_0 Connected to A
0	1	B_1 Connected to A
1	1	B_2 Connected to A





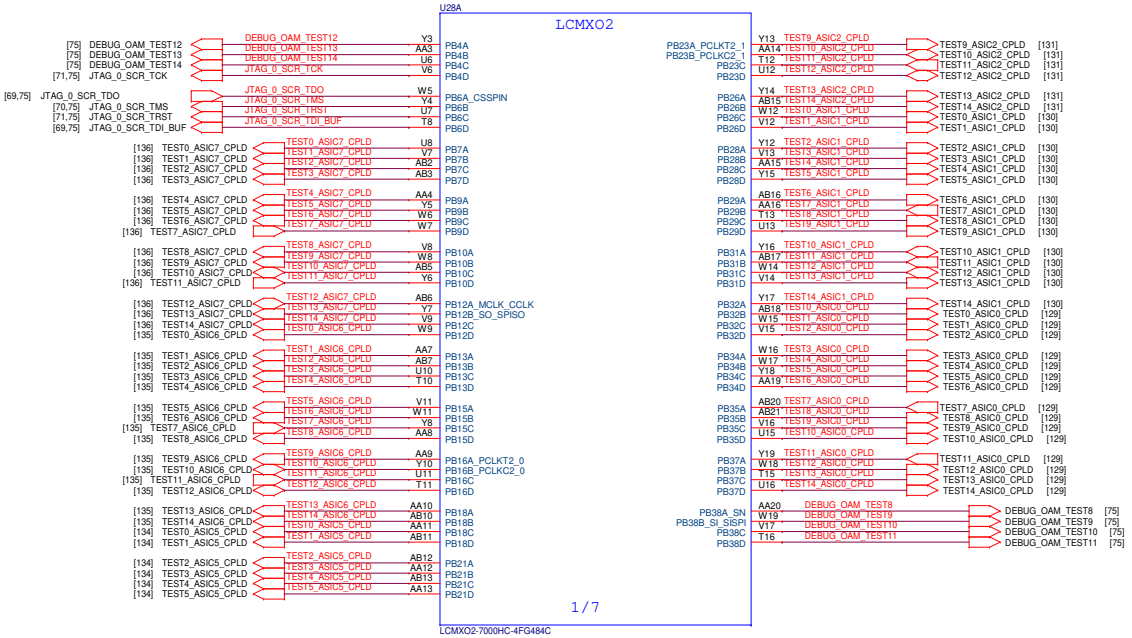


Separate LEDs (preferred)		Combined Blue/Amber LED (use only if space is limited)	Meaning(s) Communicated by each LED (one or more meanings may be valid for blue LED)	
Blue	Amber		Blue	Amber
OFF	OFF	OFF	Off/Not Functioning/Not Present. Service Action Allowed.	No Fault
ON	OFF	BLUE ON	On/Functioning, Link Established – No Activity.	No Fault
BLINK	OFF	BLUE BLINK	On/Functioning, Drive/Network Activity.	No Fault
OFF	ON	AMBER ON	Off/Not Functioning, Service Action Allowed.	Fault
OFF	BLINK	AMBER BLINK	Off/Not Functioning/Not Present. Service Action Allowed.	Locate

PFR_MUX_LED

CLKEN_OE*_N control:
When P3V3_AUX enable, CPLD set them to open drain.
If P3V3 bring up, CPLD drive low to clock buffer.

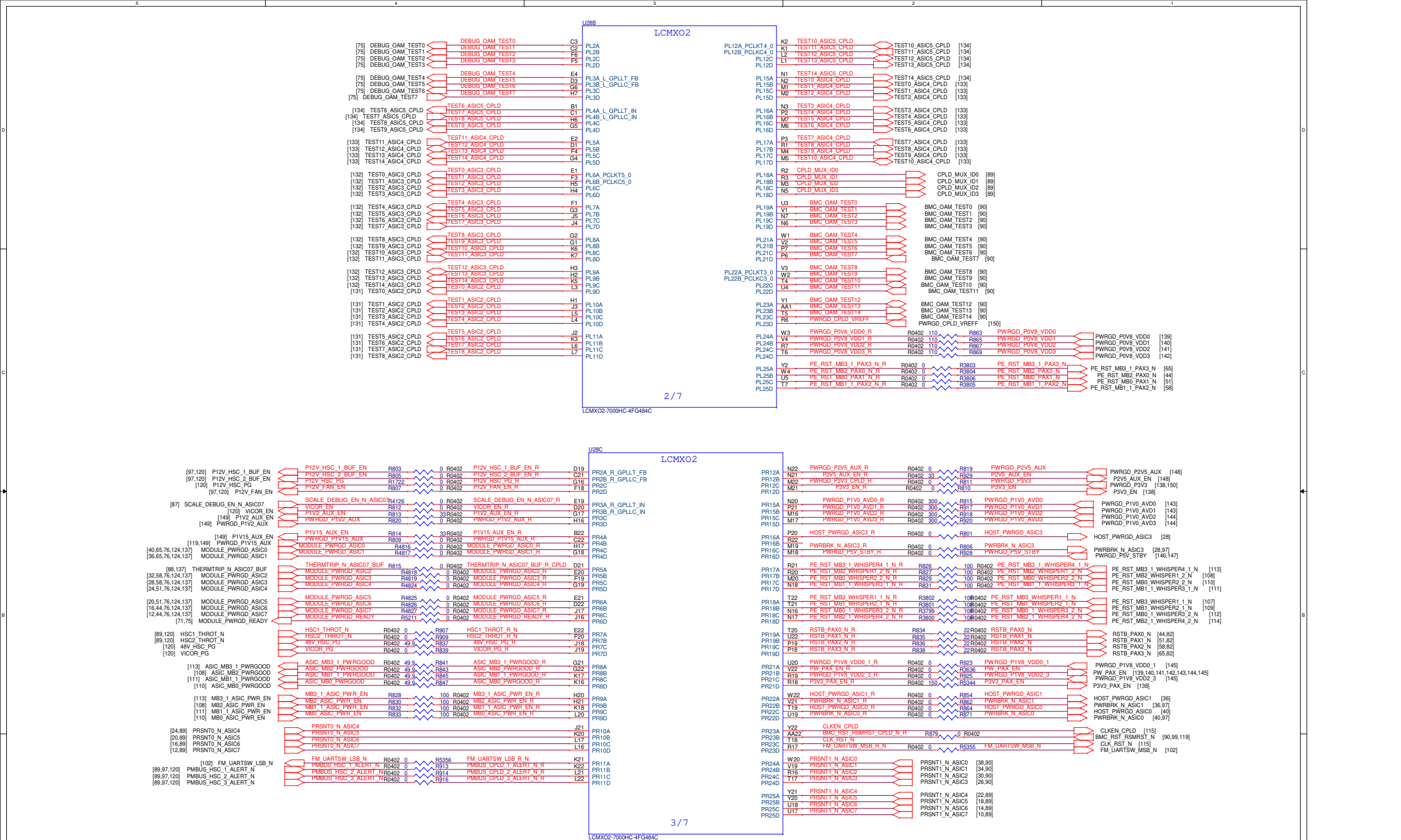
FAN_*_STATE_LED_N control:
FAN failed: FAN_*_STATE_LED = 0, FAN_*_STATE_LED_N = 0
Normal: FAN_*_STATE_LED = 1, FAN_*_STATE_LED_N = 1



RST_CPLD_RSMRST_N is CPLD chip reset.

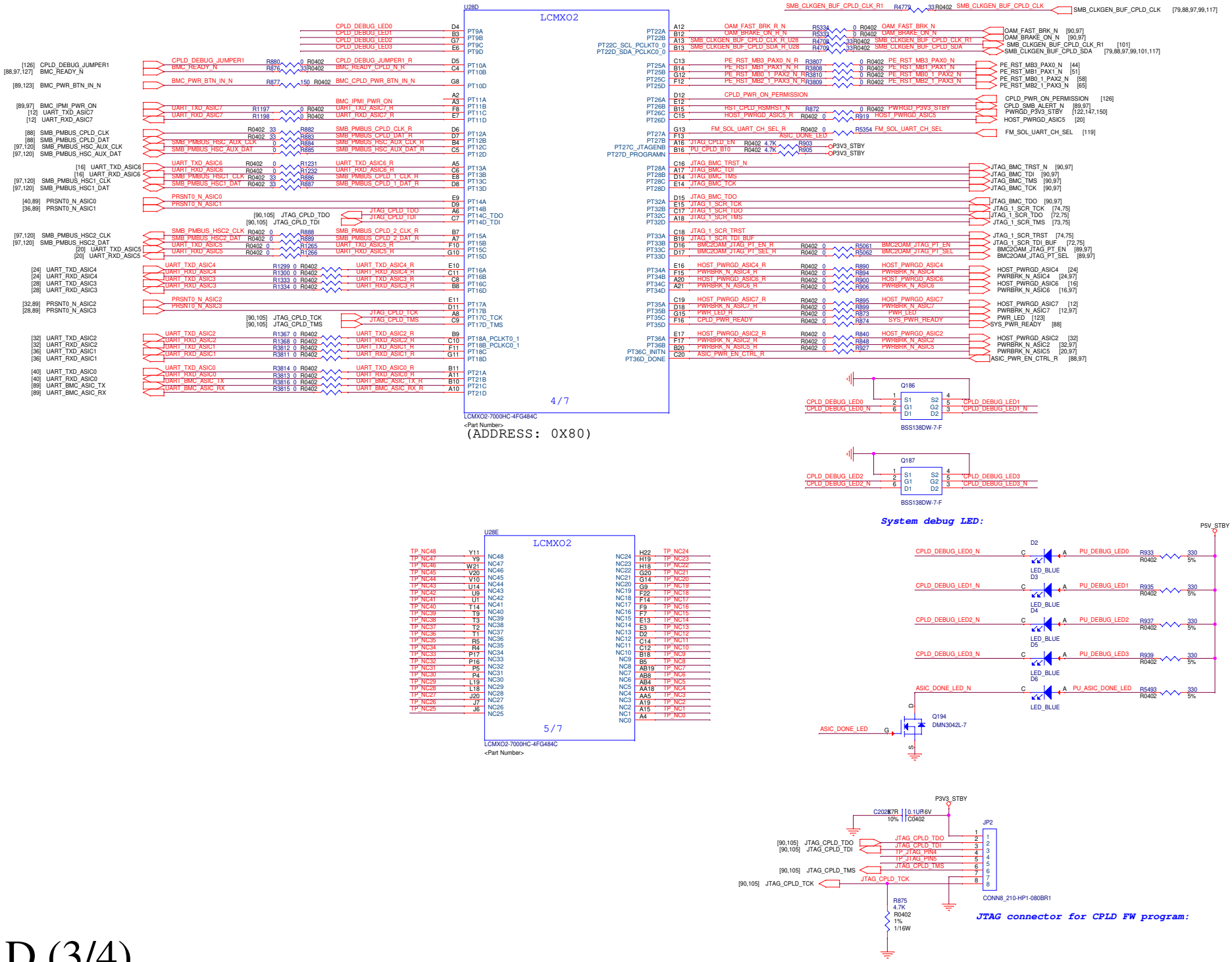
CPLD (1/4)

Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 103 of 155



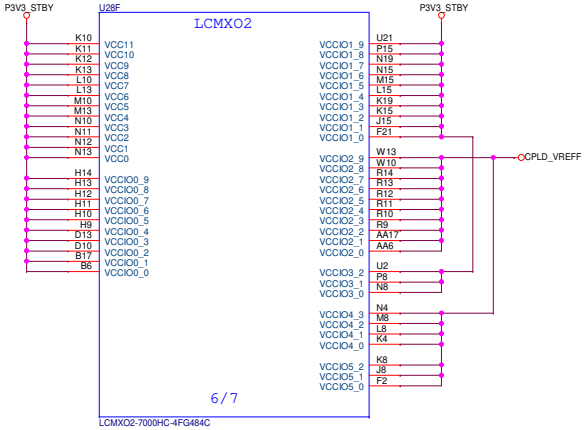
CPLD(2/4)

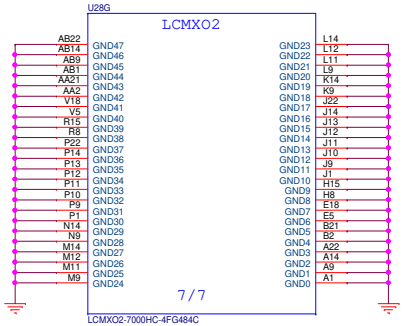
Quanta	Department: CCBU	Designer: <Designer>	Project: <project_name>	Doc Number: EP_BASEBOARD_OCP
		Reviewer: <Reviewer>	Size	Date: Tuesday, January 18, 2022
				Page Title: Cover Page
				Rev: <RevCode>
				Sheet: 104 of 155

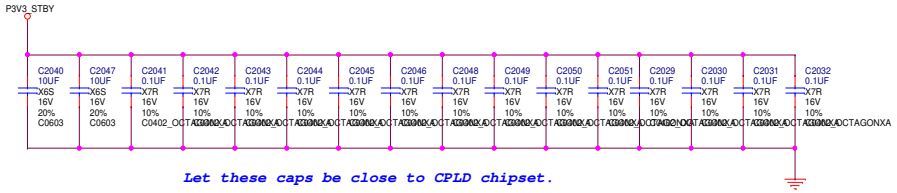


CPLD (3/4)

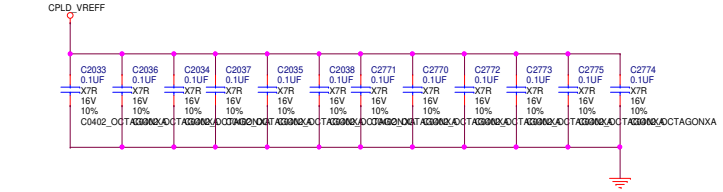
Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 105 of 155





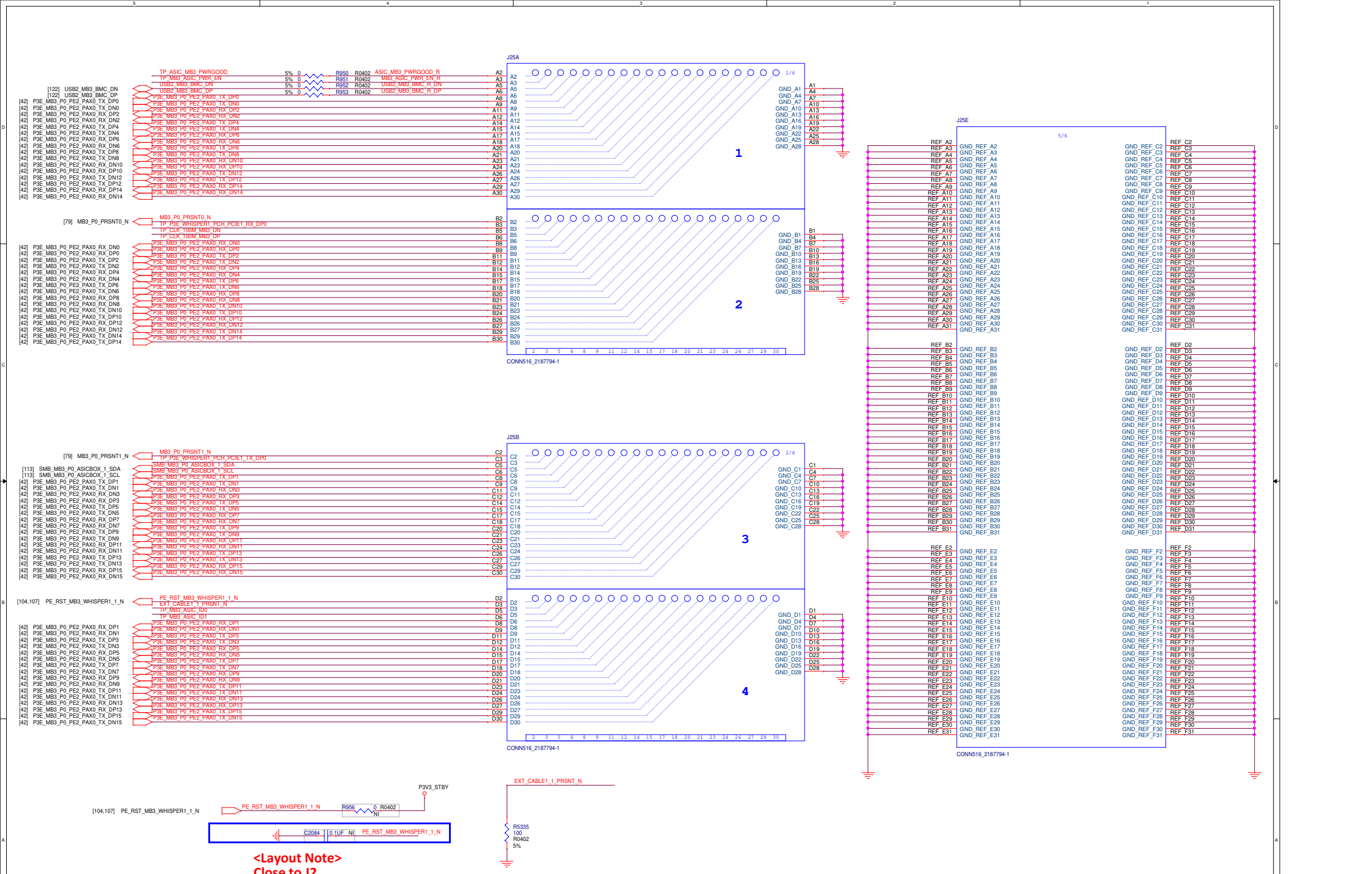


Let these caps be close to CPLD chipset.



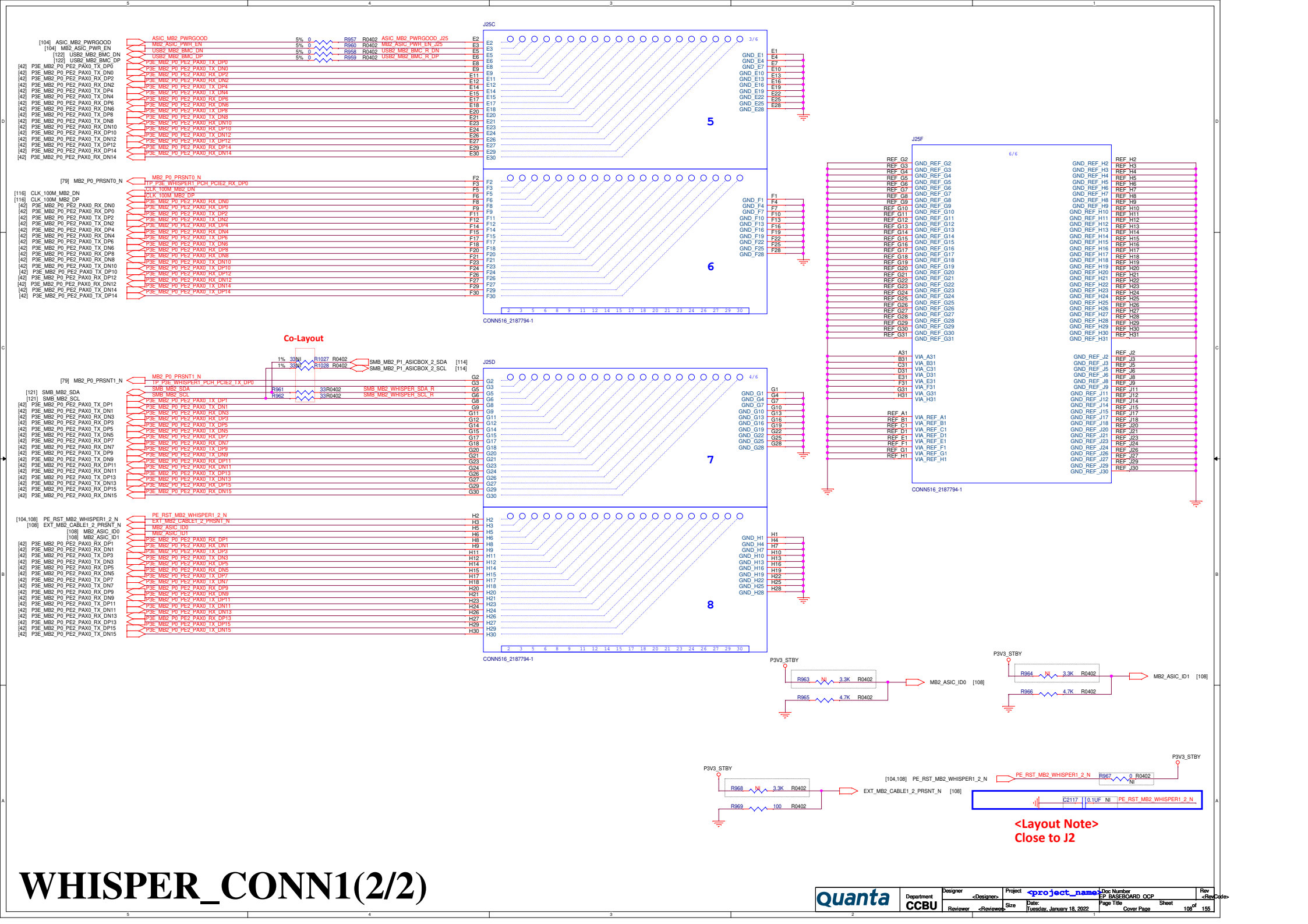
CPLD (4/4)

Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 106 of 155



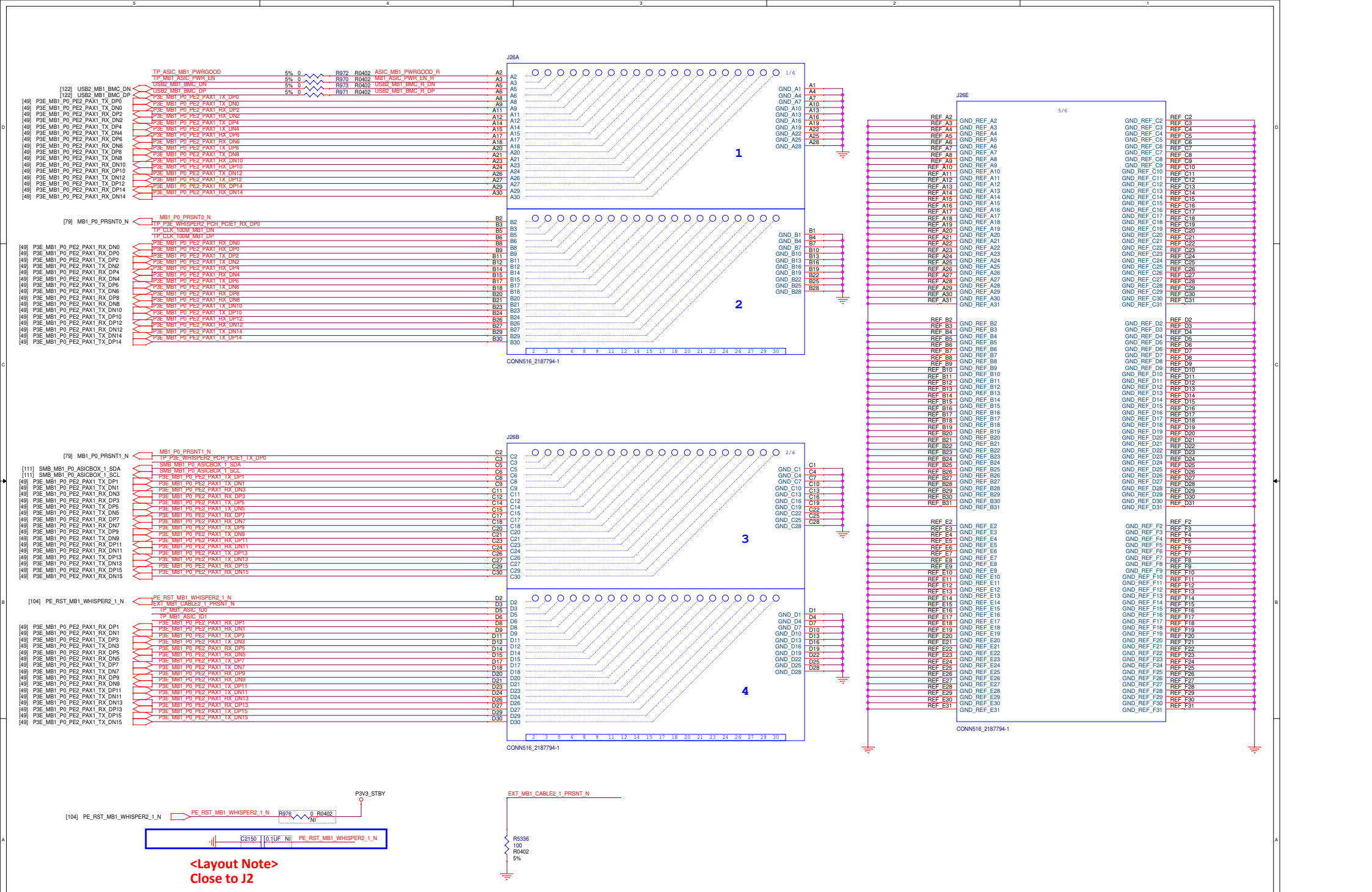
WHISPER_CONN1(1/2)

Quanta	Department: CCBU	Designer: <Designer>	Project: <project_name>	Doc Number: EP_BASEBOARD_OCP
		Reviewer: <Reviewer>	Size	Date: Tuesday, January 18, 2022
				Page Title: Cover Page
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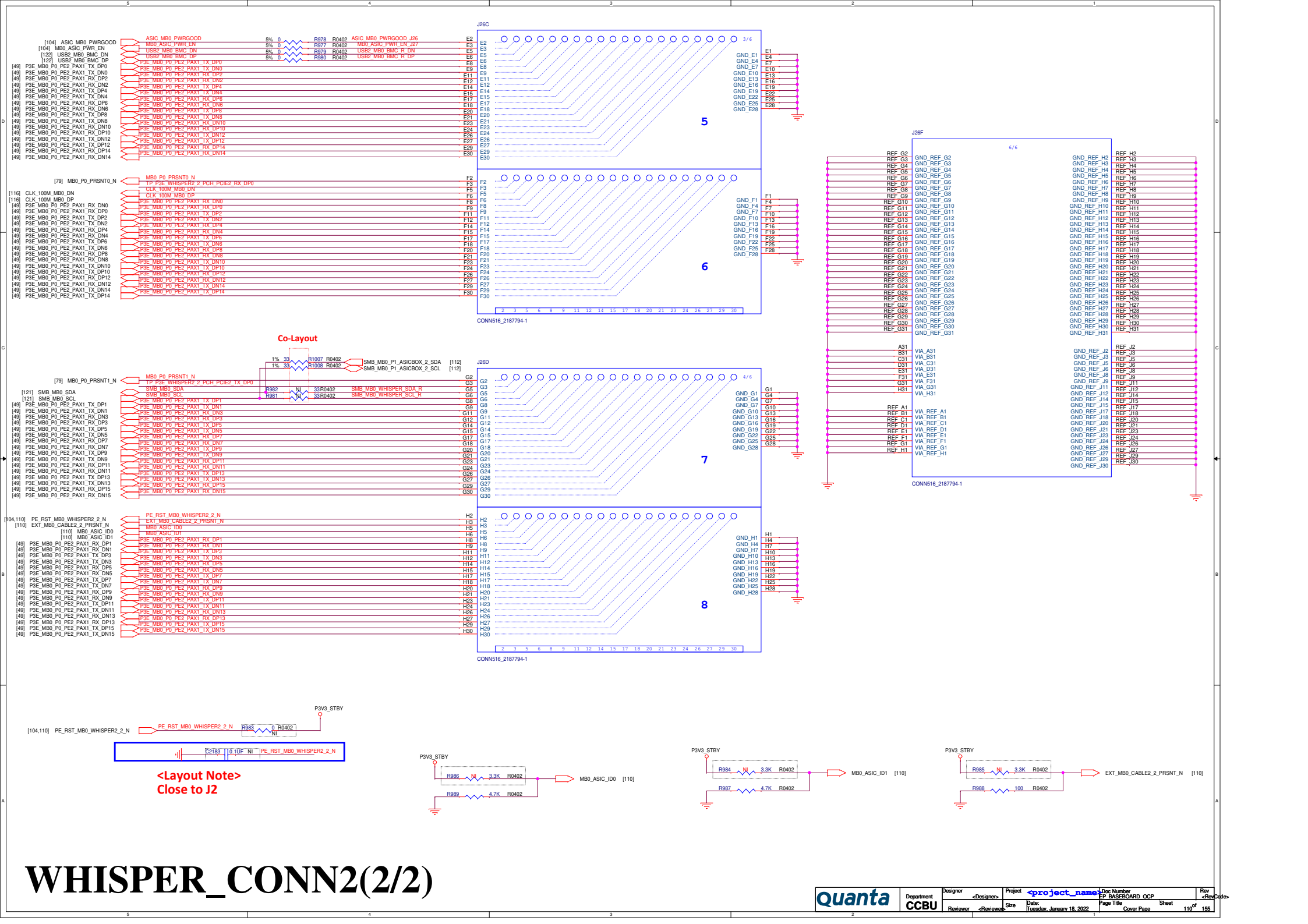
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Quanta	Department: CCBU	Designer: <Designer>	Project: <project_name>
		Reviewer: <Reviewer>	Size
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		Page Title: Cover Page	Sheet: 100 of 155
			Rev: <RevCode>



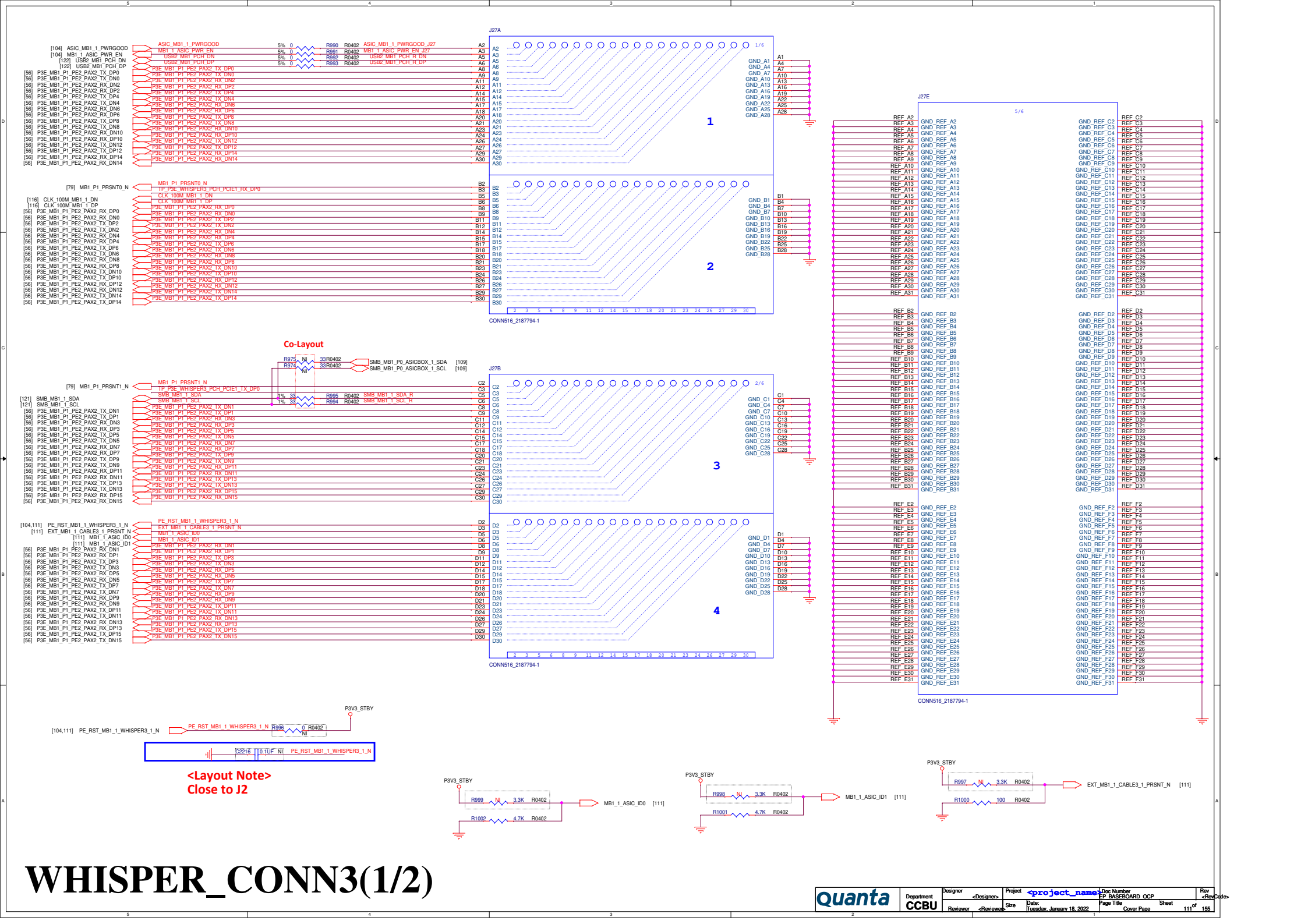
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Quanta	Department: CCBU	Designer: <Designer>	Project: <project_name>	Doc Number: EP_BASEBOARD_OCP
		Reviewer: <Reviewer>	Size	Date: Tuesday, January 18, 2022
				Page Title: Cover Page
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				Rev: <RevCode>



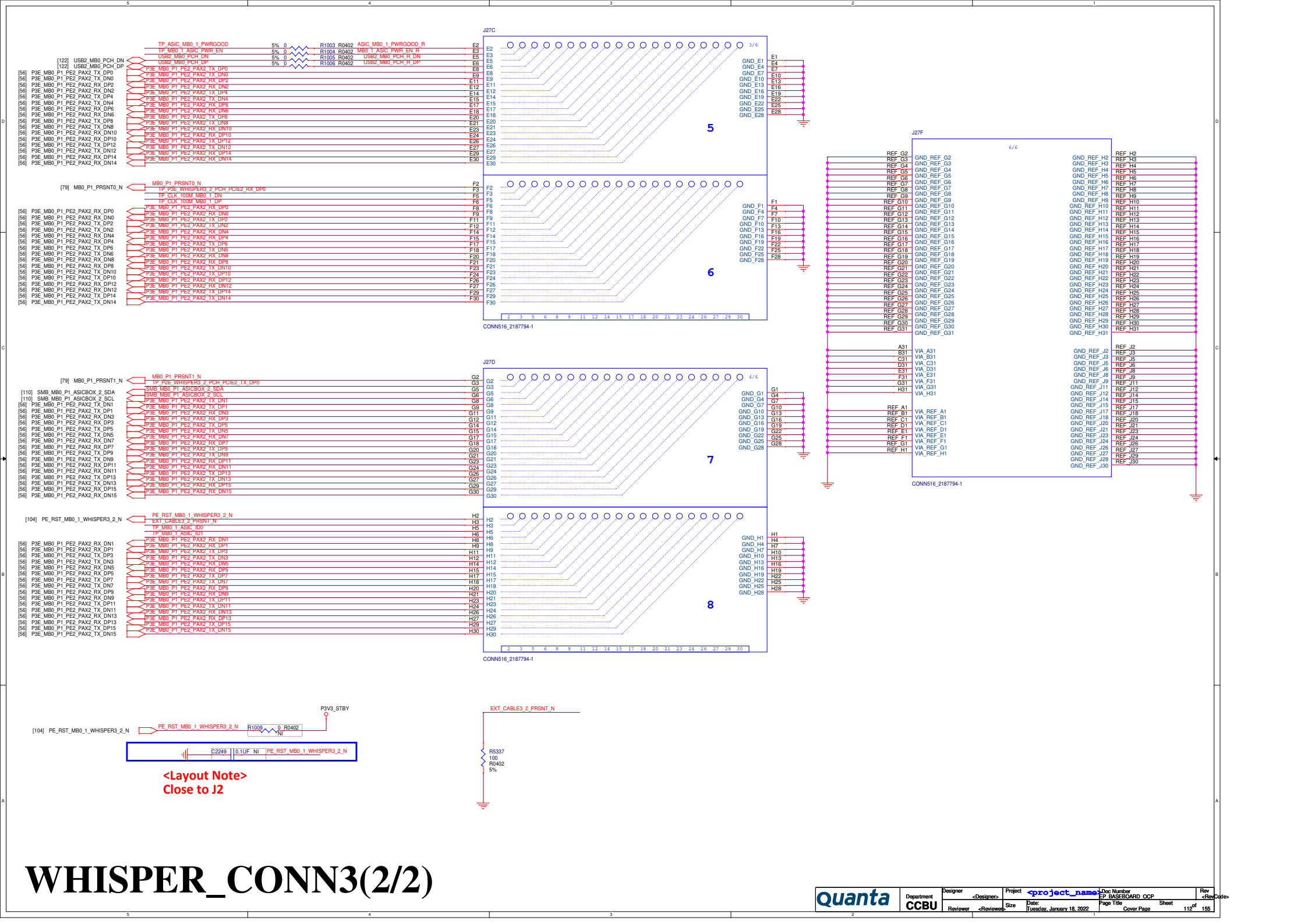
WHISPER_CONN2(2/2)

Quanta	Department: CCBU	Designer: <Designer>	Project: <project_name>	Doc Number: EP_BASEBOARD_OCP
		Reviewer: <Reviewer>	Size	Date: Tuesday, January 18, 2022
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				Rev: <RevCode>
				Sheet 110 of 155



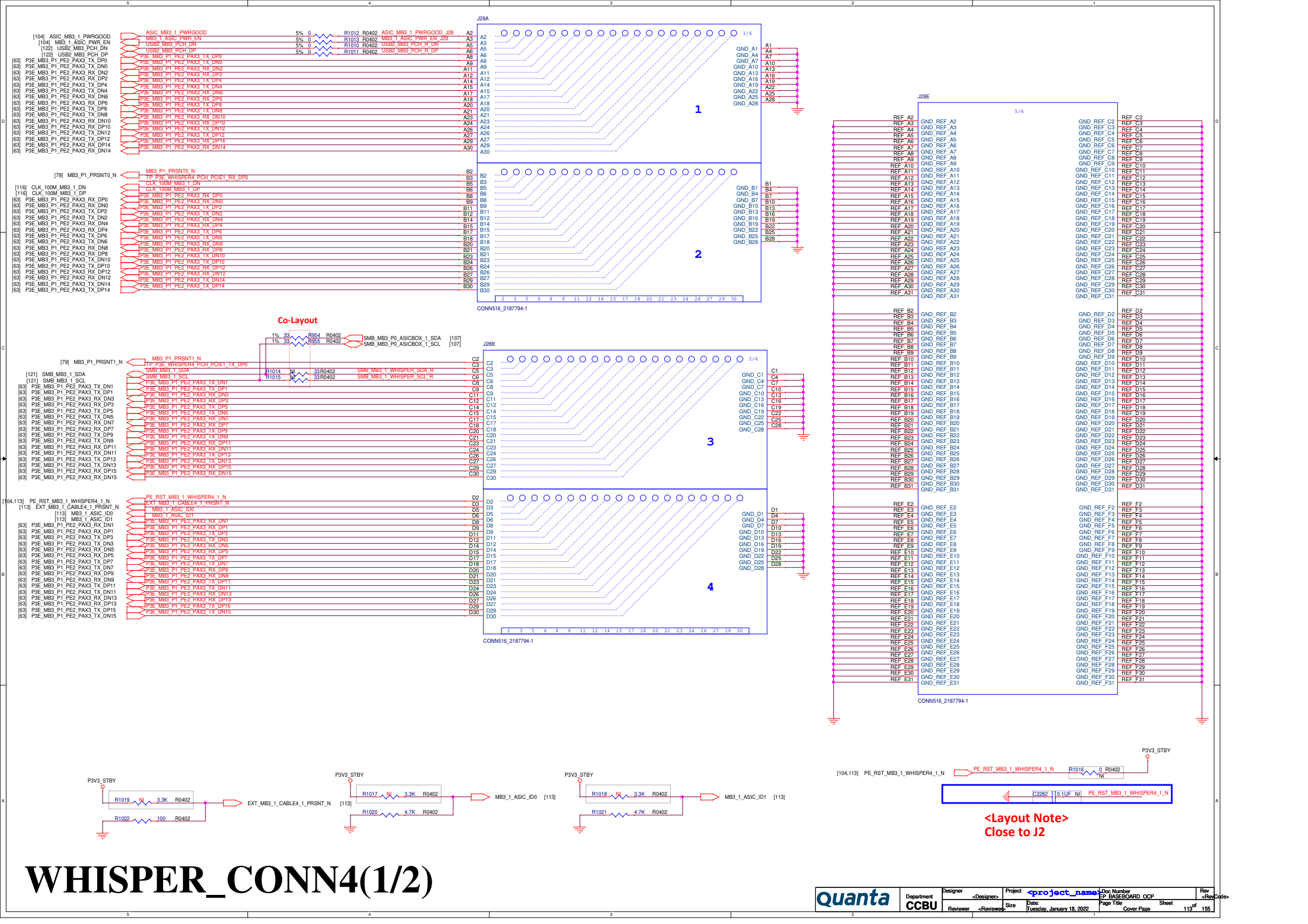
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		Reviewer: <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title: Cover Page — Sheet 111 of 155



WHISPER_CONN3(2/2)

Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022
				Page Title Cover Page
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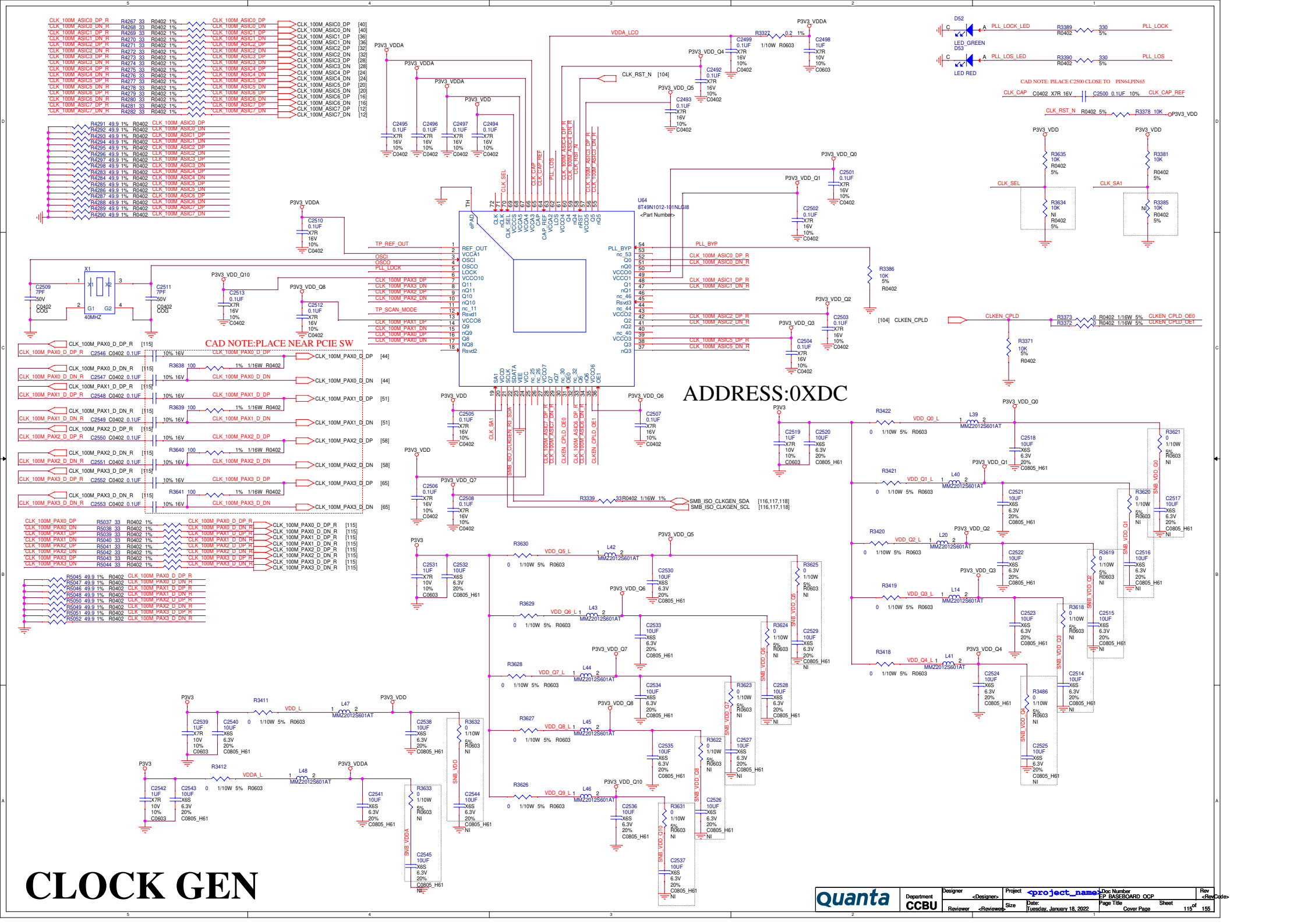


WHISPER_CONN4(1/2)

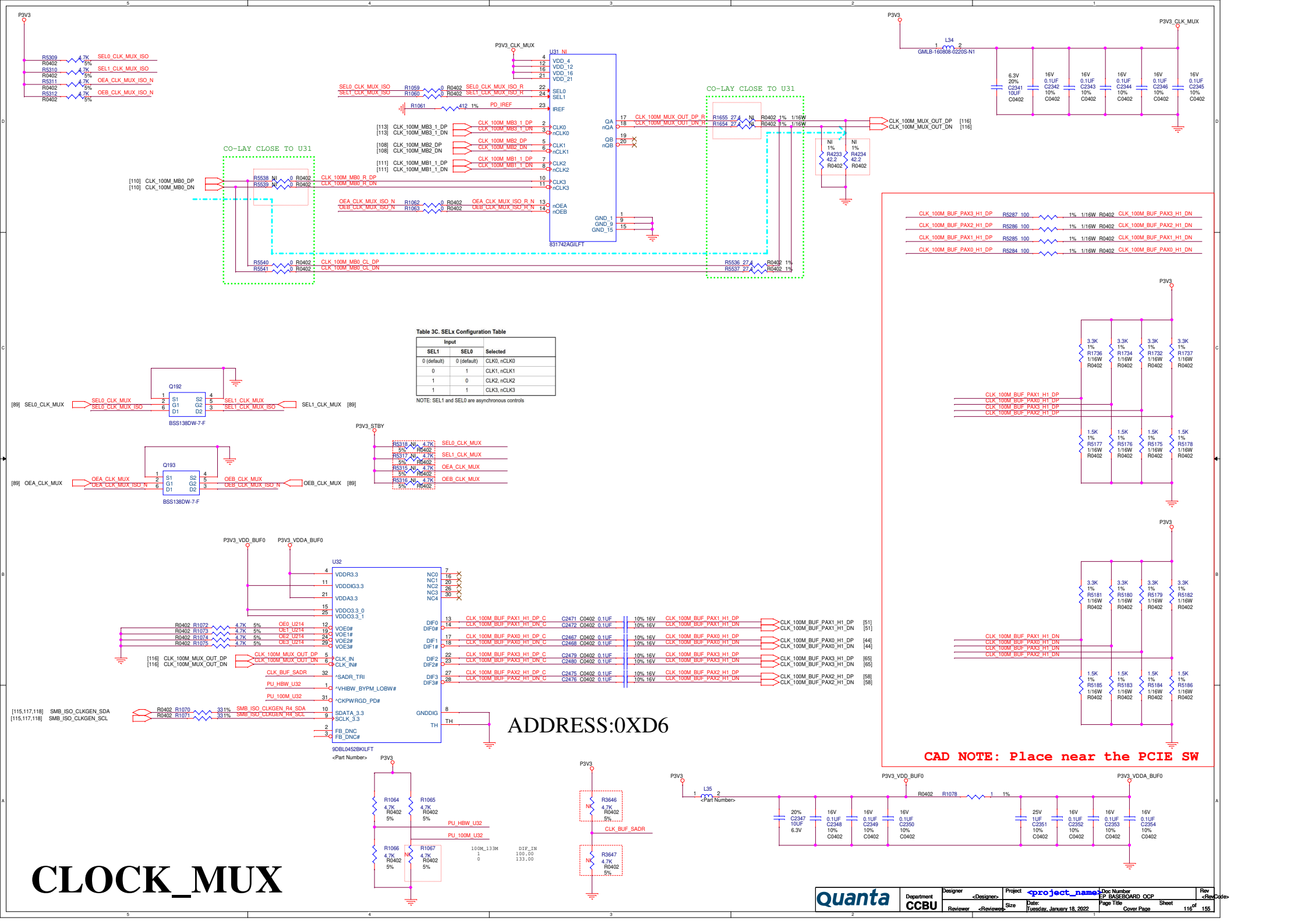
Quanta	Department: CCBU	Designer: <Designer>	Project: <project_name>
		Reviewer: <Reviewer>	Size
		Date: Tuesday, January 18, 2022	Doc Number: EP_BASEBOARD_OCP
		Page Title: Cover Page	Sheet: 113 of 155
			Rev: <RevCode>

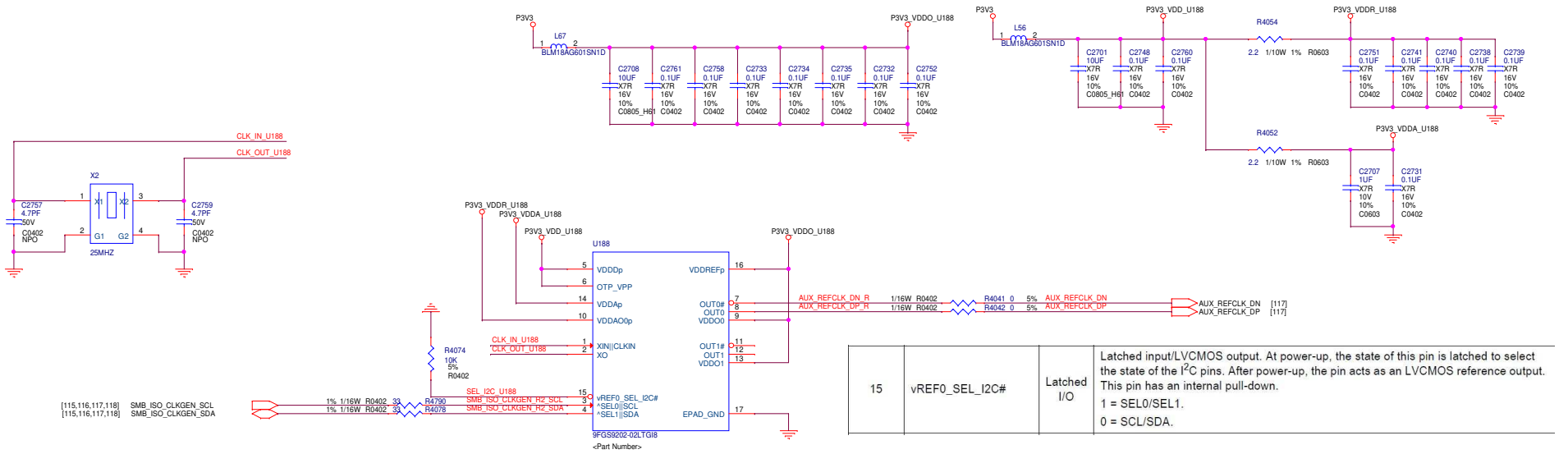
WHISPER_CONN4(2/2)

Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 114 of 155



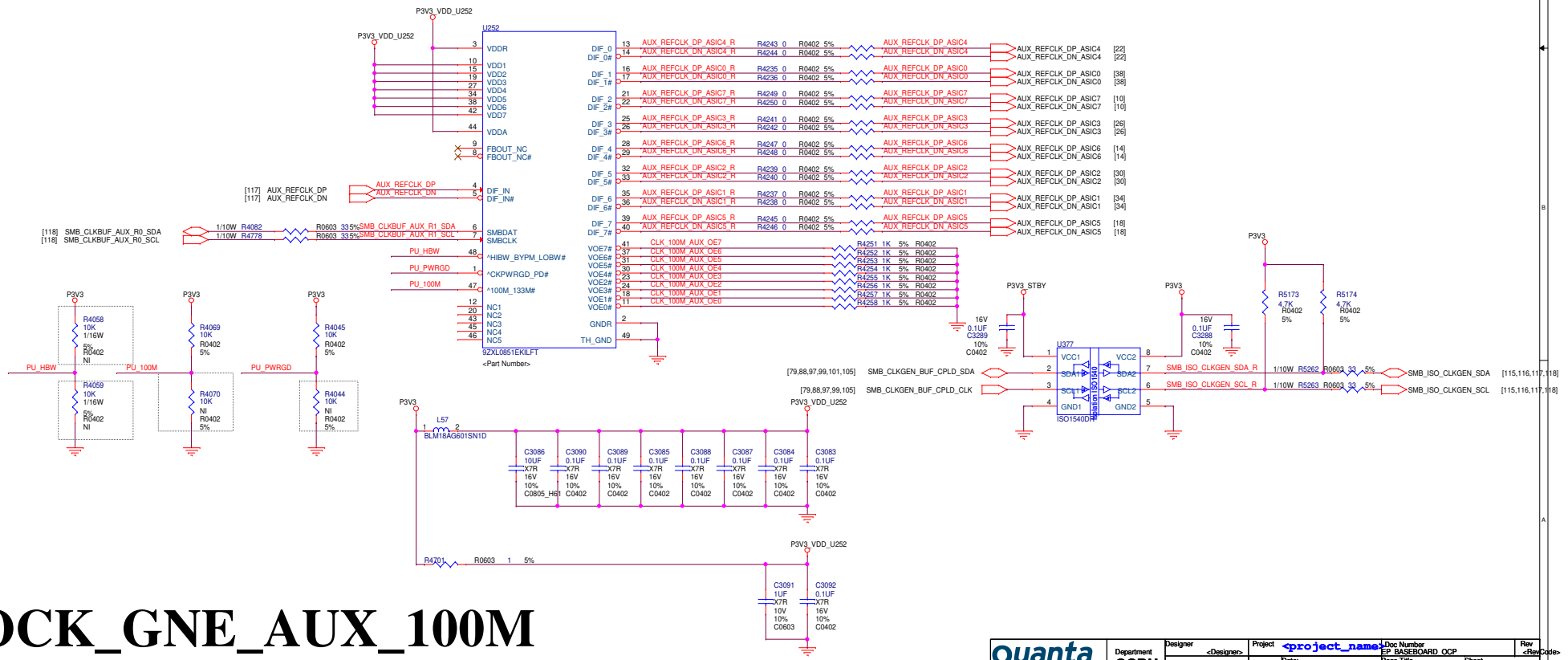
Quanta	Department: CCBU	Designer: <Designer>	Project: <project_name>
		Reviewer: <Reviewer>	Size
		Date: Tuesday, January 18, 2022	Sheet: 115 of 155
Doc Number: EP BASEBOARD_OCP	Rev: <RevCode>	Page Title: Cover Page	


P3V3
P3V3_CLK_MUX
U31_NI
831742AGILFT
CO-LAY CLOSE TO U31
CO-LAY CLOSE TO U31
L34
GMLB-160808-0220S-N1
L35
<Part Number>
SEL0_CLK_MUX_ISO
SEL1_CLK_MUX_ISO
OEA_CLK_MUX_ISO_N
OEB_CLK_MUX_ISO_N
CLK_100M_MUX_OUT_DP
CLK_100M_MUX_OUT_DN
CLK_100M_MB0_R_DP
CLK_100M_MB0_R_DN
CLK_100M_MB0_CL_DP
CLK_100M_MB0_CL_DN
CLK_100M_MB3_1_DP
CLK_100M_MB3_1_DN
CLK_100M_MB2_DP
CLK_100M_MB2_DN
CLK_100M_MB1_1_DP
CLK_100M_MB1_1_DN
CLK_100M_BUF_PAX3_H1_DP
CLK_100M_BUF_PAX2_H1_DP
CLK_100M_BUF_PAX1_H1_DP
CLK_100M_BUF_PAX0_H1_DP
Table 3C. SELx Configuration Table
Input
SEL1
SEL0
Selected
0 (default)
0 (default)
CLK0, nCLK0
0
1
CLK1, nCLK1
1
0
CLK2, nCLK2
1
1
CLK3, nCLK3
NOTE: SEL1 and SEL0 are asynchronous controls
Q192
Q193
BSS138DW-7-F
P3V3_STBY
P3V3_VDD_BUF0
P3V3_VDDA_BUF0
U32
9DBL0452BKILFT
ADDRESS:0XD6
CAD NOTE: Place near the PCIE SW
CLOCK_MUX
Quanta
Department
CCBU
Designer
<Designer>
Reviewer
<Reviewer>
Project
<project_name>
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Date:
Tuesday, January 18, 2022
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155

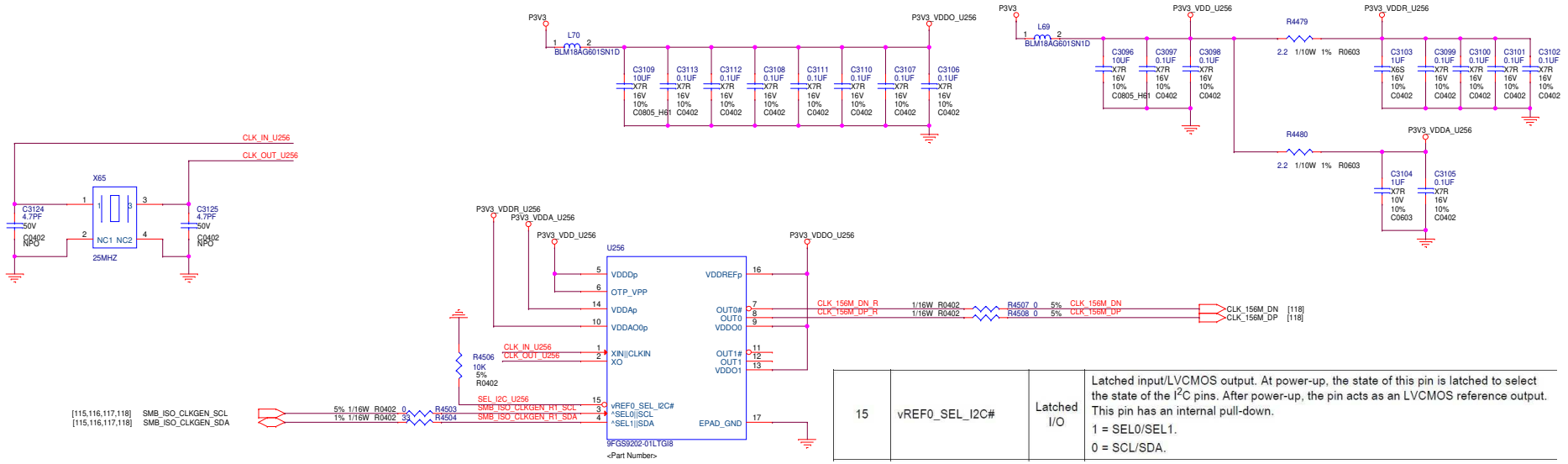


15	vREF0_SEL_I2C#	Latched I/O	Latched input/LVCMOS output. At power-up, the state of this pin is latched to select the state of the I²C pins. After power-up, the pin acts as an LVCMOS reference output. This pin has an internal pull-down. 1 = SEL0/SEL1. 0 = SCL/SDA.

ADDRESS:0XD4

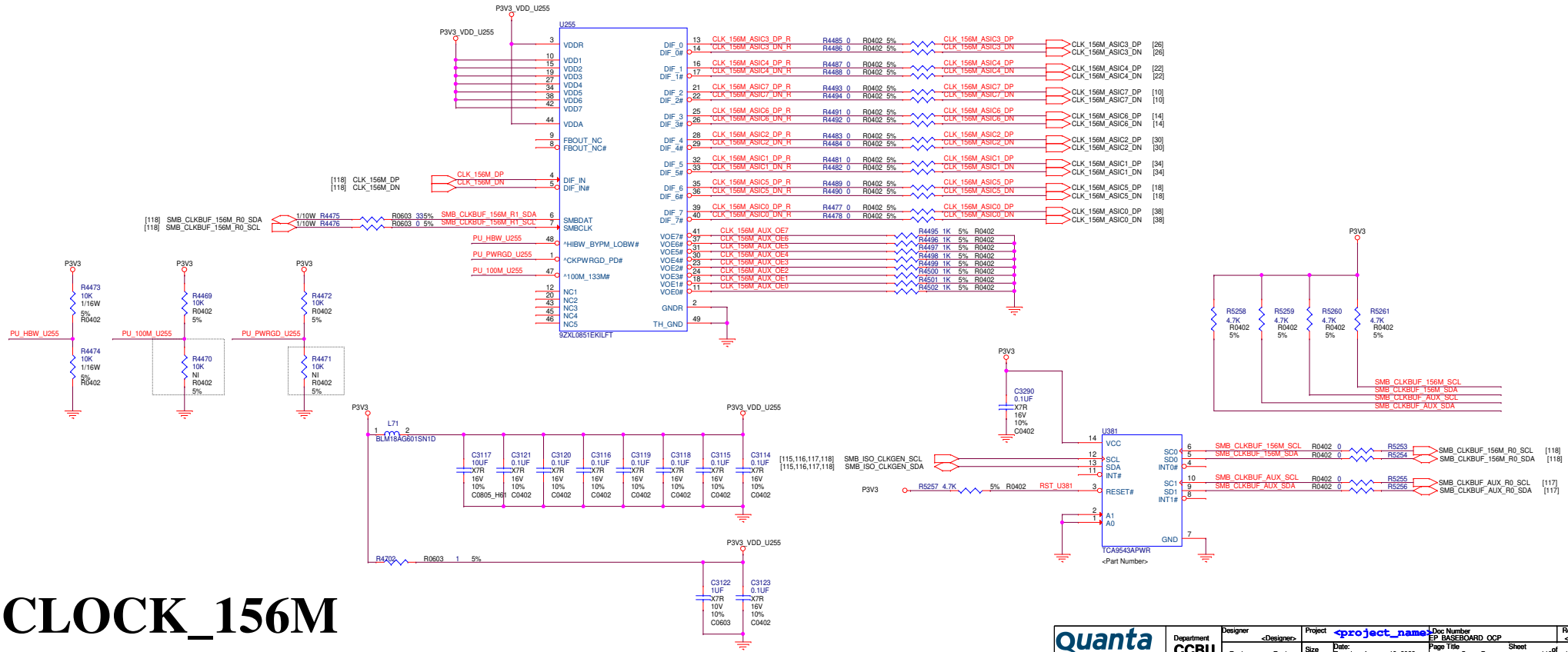


CLOCK_GNE_AUX_100M

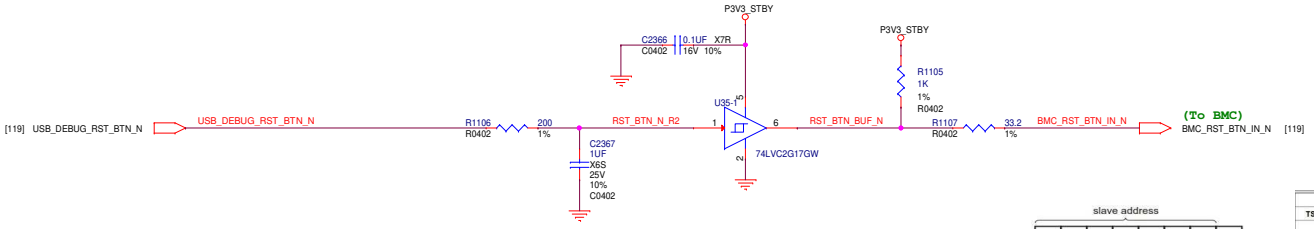


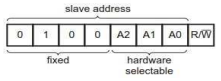
15	vREF0_SEL_I2C#	Latched I/O	Latched input/LVCMOS output. At power-up, the state of this pin is latched to select the state of the I^2C pins. After power-up, the pin acts as an LVCMOS reference output. This pin has an internal pull-down. 1 = SEL0/SEL1. 0 = SCL/SDA.

ADDRESS:0XD0



CLOCK_156M





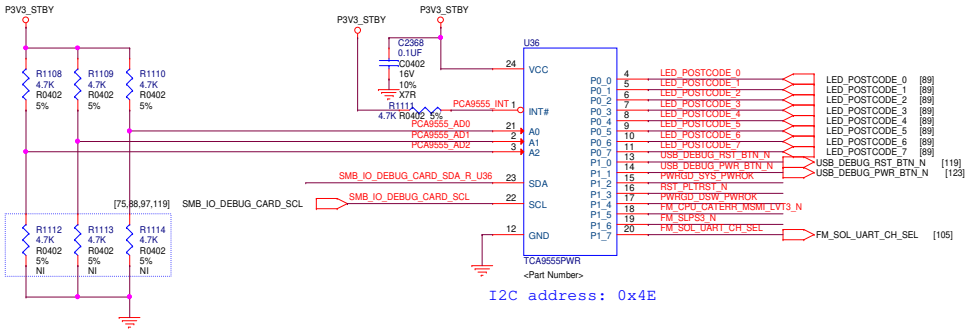
[75,88,97,119] SMB_IO_DEBUG_CARD_SDA SMB_IO_DEBUG_CARD_SDA R1124 33R0402 SMB_IO_DEBUG_CARD_SDA_R_U36

GPIO expander for Debug Card V2

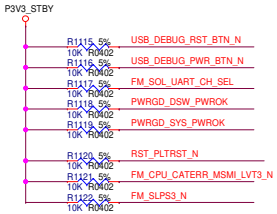
IO BD Address Setting

0	1	0	0	1	1	1

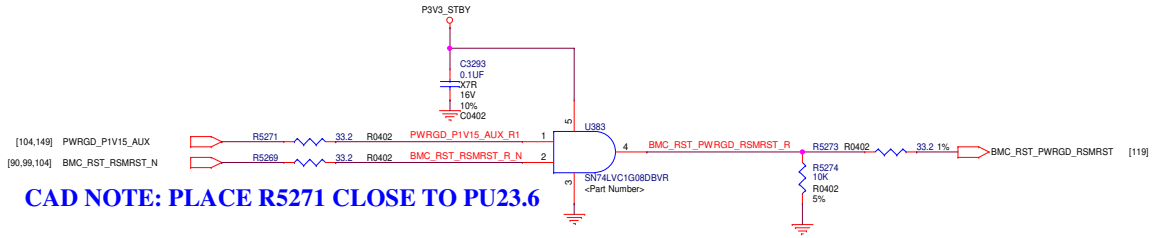
Fix on IO board



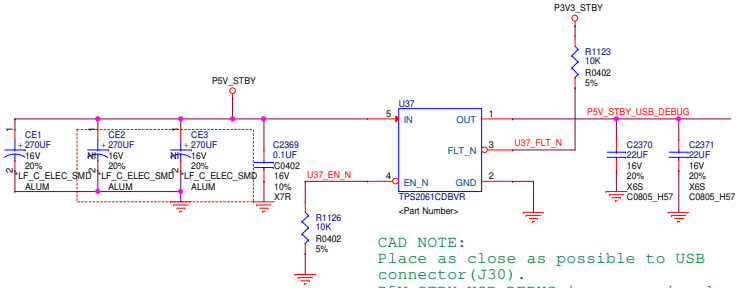
I2C address: 0x4E



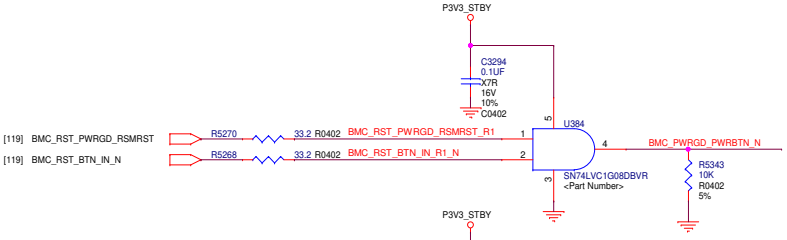
NO. TSSOP (PW)	NO. QFN (RTW)	NAME	DESCRIPTION
1	22	$\overline{INT}$	Interrupt output. Connect to V_{CC} through a pullup resistor.
2	23	A1	Address input 1. Connect directly to V_{CC} or ground.
3	24	A2	Address input 2. Connect directly to V_{CC} or ground.
4	1	P00	P-port input/output. Push-pull design structure. At power on, P00 is configured as an input.
5	2	P01	P-port input/output. Push-pull design structure. At power on, P01 is configured as an input.
6	3	P02	P-port input/output. Push-pull design structure. At power on, P02 is configured as an input.
7	4	P03	P-port input/output. Push-pull design structure. At power on, P03 is configured as an input.
8	5	P04	P-port input/output. Push-pull design structure. At power on, P04 is configured as an input.
9	6	P05	P-port input/output. Push-pull design structure. At power on, P05 is configured as an input.
10	7	P06	P-port input/output. Push-pull design structure. At power on, P06 is configured as an input.
11	8	P07	P-port input/output. Push-pull design structure. At power on, P07 is configured as an input.
12	9	GND	Ground
13	10	P10	P-port input/output. Push-pull design structure. At power on, P10 is configured as an input.
14	11	P11	P-port input/output. Push-pull design structure. At power on, P11 is configured as an input.
15	12	P12	P-port input/output. Push-pull design structure. At power on, P12 is configured as an input.
16	13	P13	P-port input/output. Push-pull design structure. At power on, P13 is configured as an input.
17	14	P14	P-port input/output. Push-pull design structure. At power on, P14 is configured as an input.
18	15	P15	P-port input/output. Push-pull design structure. At power on, P15 is configured as an input.
19	16	P16	P-port input/output. Push-pull design structure. At power on, P16 is configured as an input.
20	17	P17	P-port input/output. Push-pull design structure. At power on, P17 is configured as an input.
21	18	A0	Address input 0. Connect directly to V_{CC} or ground.
22	19	SCL	Serial clock bus. Connect to V_{CC} through a pullup resistor.
23	20	SDA	Serial data bus. Connect to V_{CC} through a pullup resistor.
24	21	V_{CC}	Supply voltage

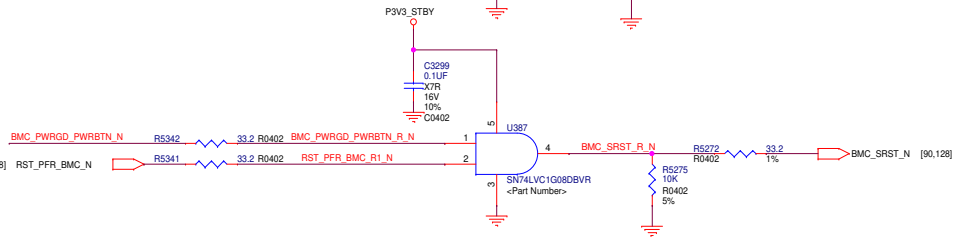


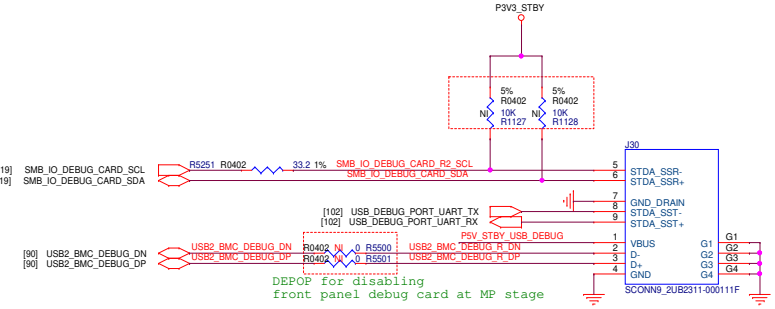
CAD NOTE: PLACE R5271 CLOSE TO PU23.6



CAD NOTE:
Place as close as possible to USB connector(J30).
P5V_STBY_USB_DEBUG is power signal need use power shape.







DEPOP for disabling front panel debug card at MP stage

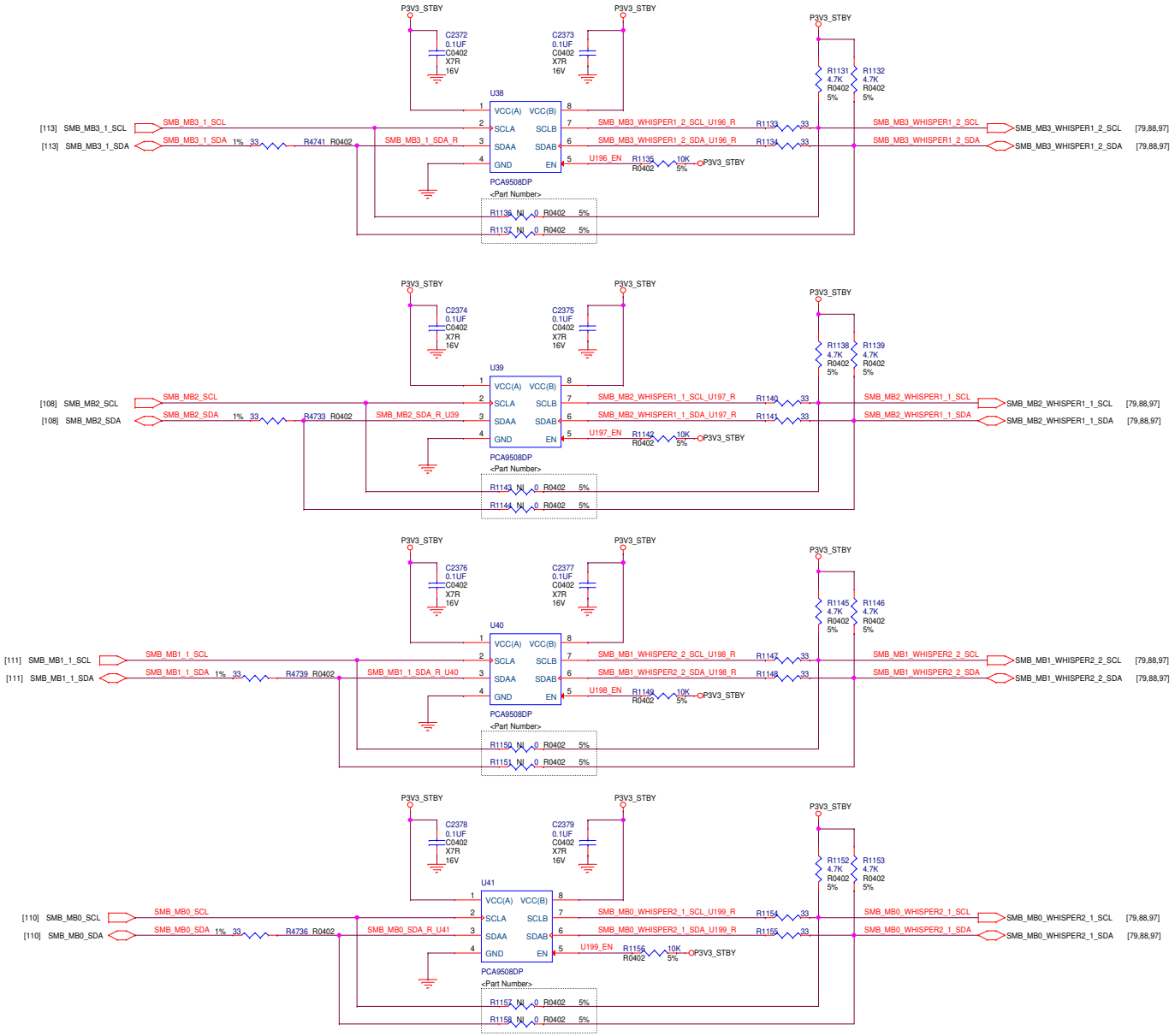
USB DEBUG

Quanta	Department	Designer	Project	Doc Number	Rev
	CCBU	<Designer>	<project_name>	EP BASEBOARD OCP	<RevCode>
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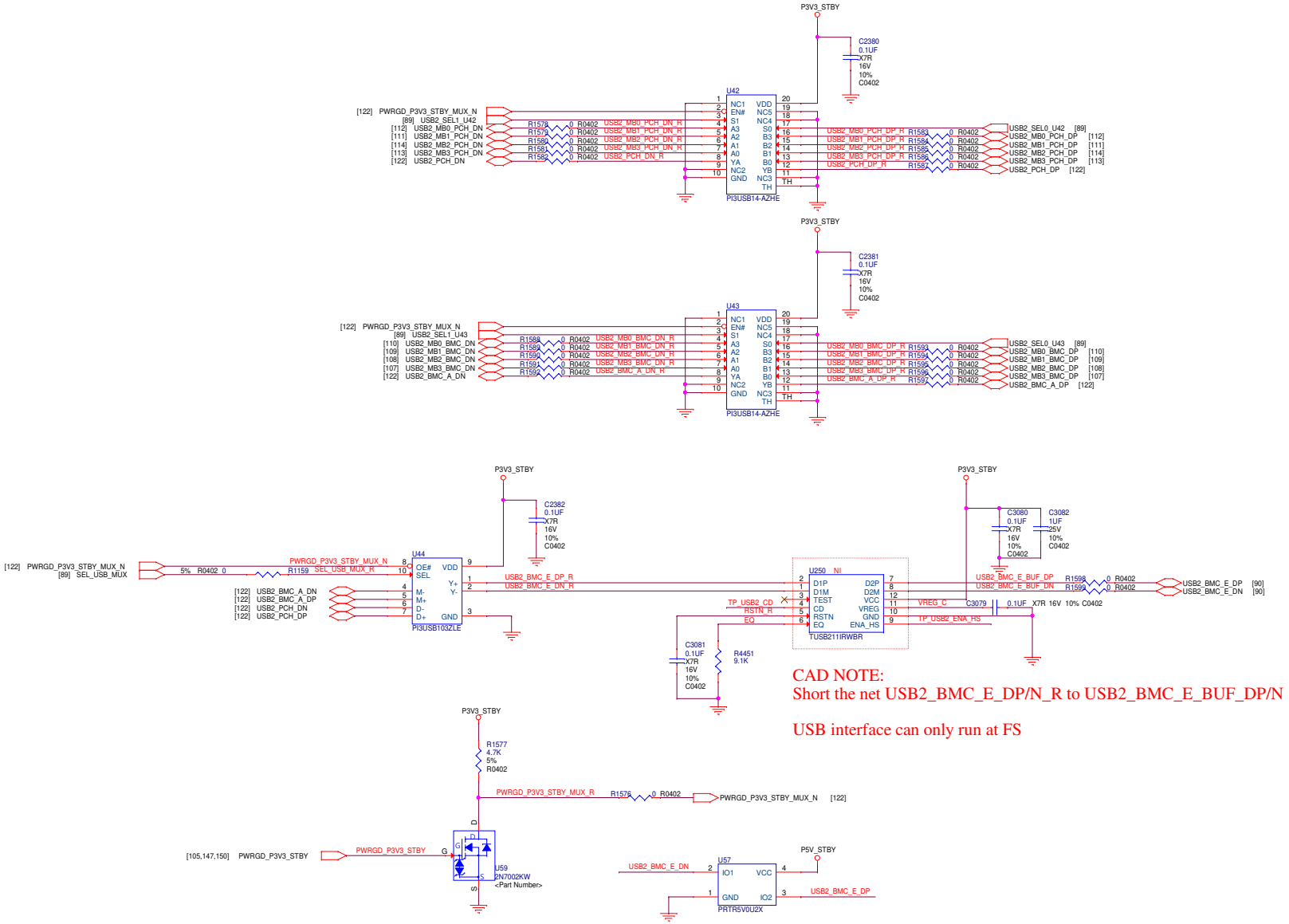
PWR CONN

Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 120 of 155



REPEATER

Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 121 of 155

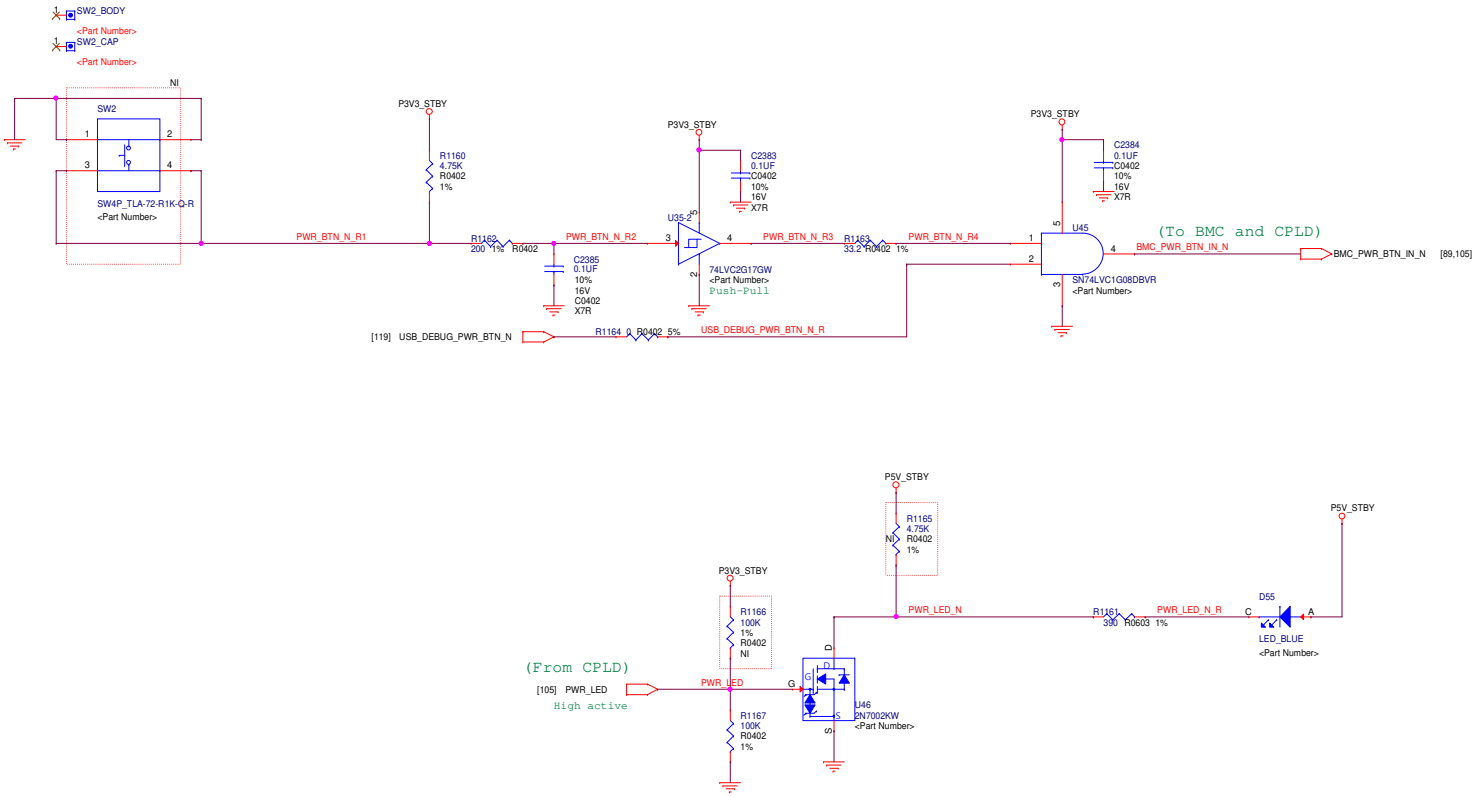


CAD NOTE:
Short the net USB2_BMC_E_DP/N_R to USB2_BMC_E_BUF_DP/N

USB interface can only run at FS

USB MUX

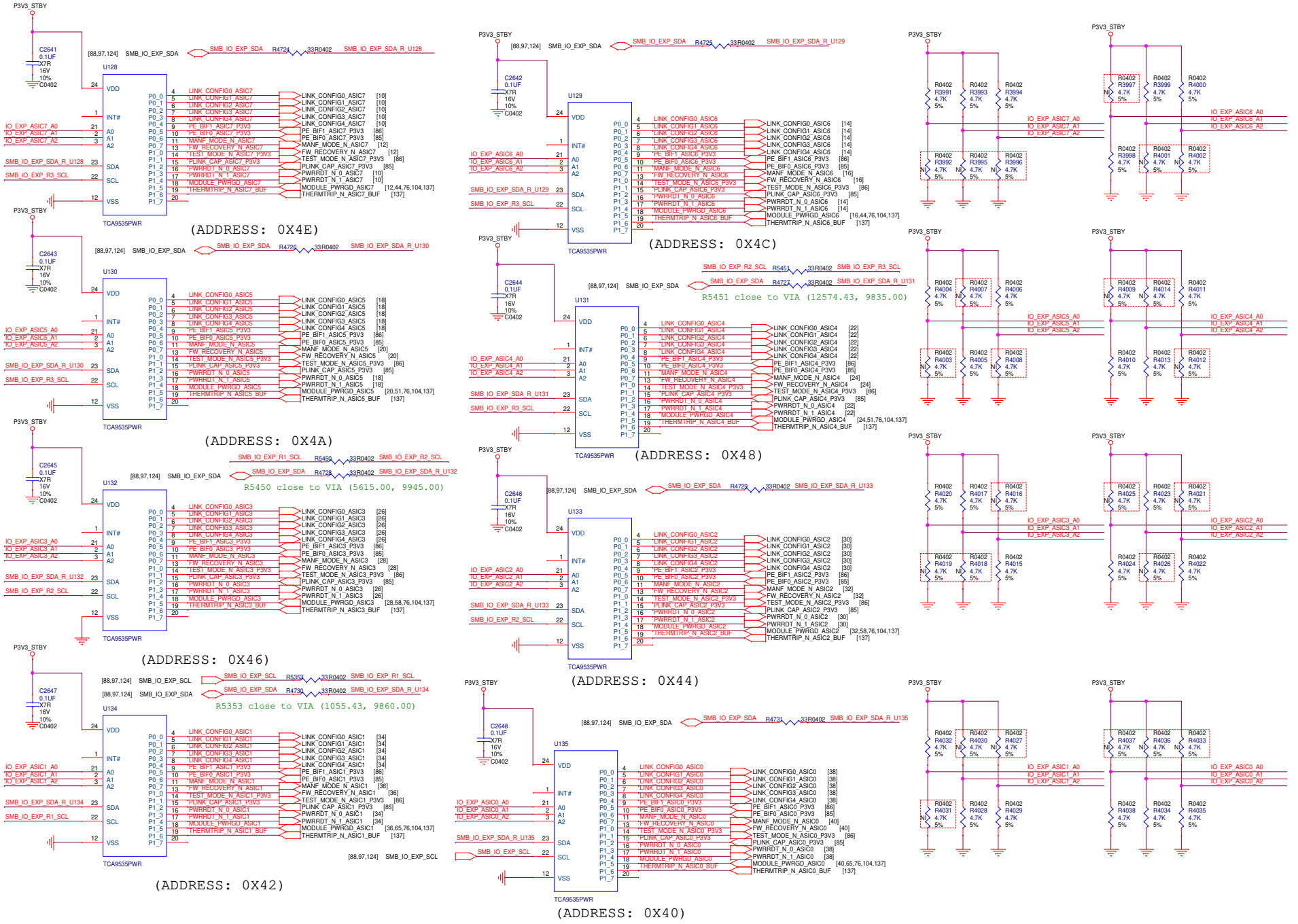
Quanta	Department CCBU	Designer <Designer>	Project <project_name>	Doc Number EP_BASEBOARD_OCP	Rev <RevCode>
		Reviewer <Reviewer>	Size	Date: Tuesday, January 18, 2022	Page Title Cover Page Sheet 122 of 155



4. Electrical / Optical Characteristics at TA=25℃

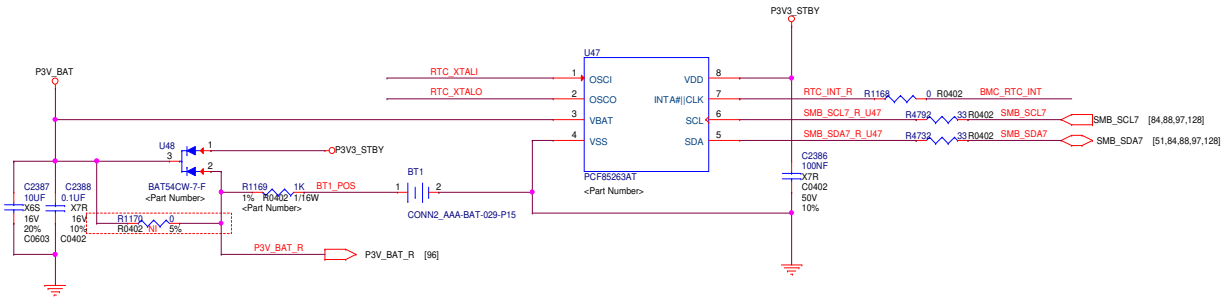
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Luminous Intensity	IV	4.5	-	29	mcd	IF = 10mA Note 1, 5
Viewing Angle	2θ1/2		40		deg	Note 2 (Fig.6)
Peak Emission Wavelength	λP		468		nm	Measurement @Peak (Fig.1)
Dominant Wavelength	λd	464	470	477	nm	IF=10 mA, Note 4
Spectral Line Half-Width	Δλ		20		nm	
Forward Voltage	VF		3.1	3.8	V	IF = 10mA
Reverse Current	IR			10	μA	VR = 5V, Note 6

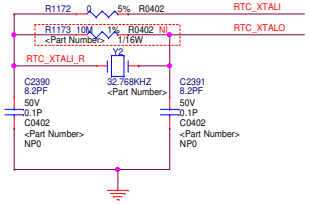
PWR_BUTTON

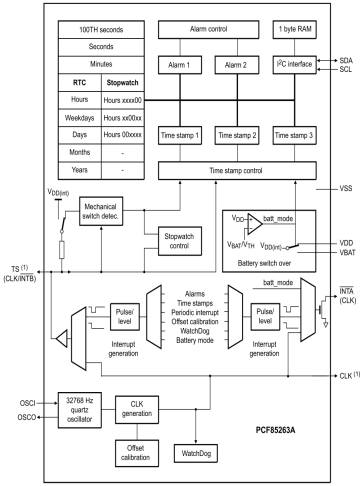


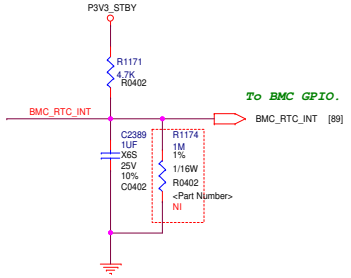
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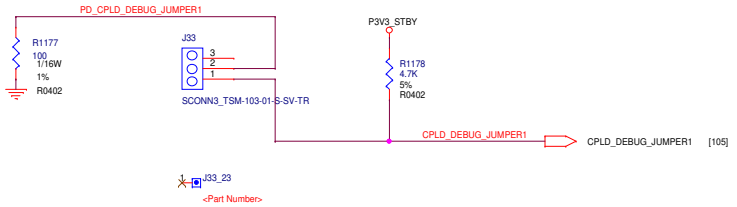


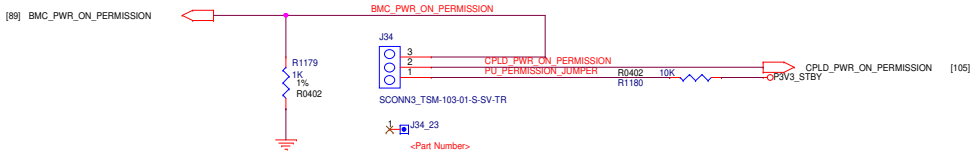


I2C_RTC_IC

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CPLD DEBUG HEADER



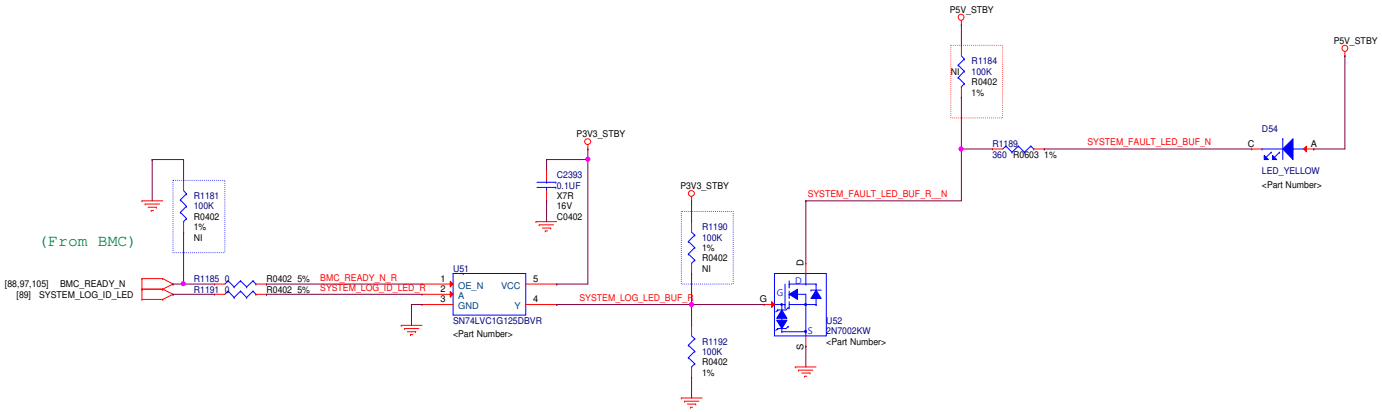


BMC&CPLD DEBUG HEADER

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4. Electrical / Optical Characteristics at TA=25℃

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Luminous Intensity	IV	4.5		38	mcd	IF = 20mA Note 1, 3
Viewing Angle	2θ1/2		40		deg	Note 2 (Fig.6)
Peak Emission Wavelength	λP		592		nm	Measurement @Peak (Fig.1)
Dominant Wavelength	λd	582	589	595	nm	IF=20 mA, Note 4
Spectral Line Half-Width	Δλ		15		nm	
Forward Voltage	VF		2.0	2.5	V	IF = 20mA
Reverse Current	IR			10	μA	VR = 5V, Note 5

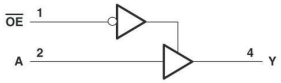


ID	System Log	Color	Behavior
Not Located	N/A	Yellow	OFF
Not Located	Fault		ON
Located	N/A		BLINK

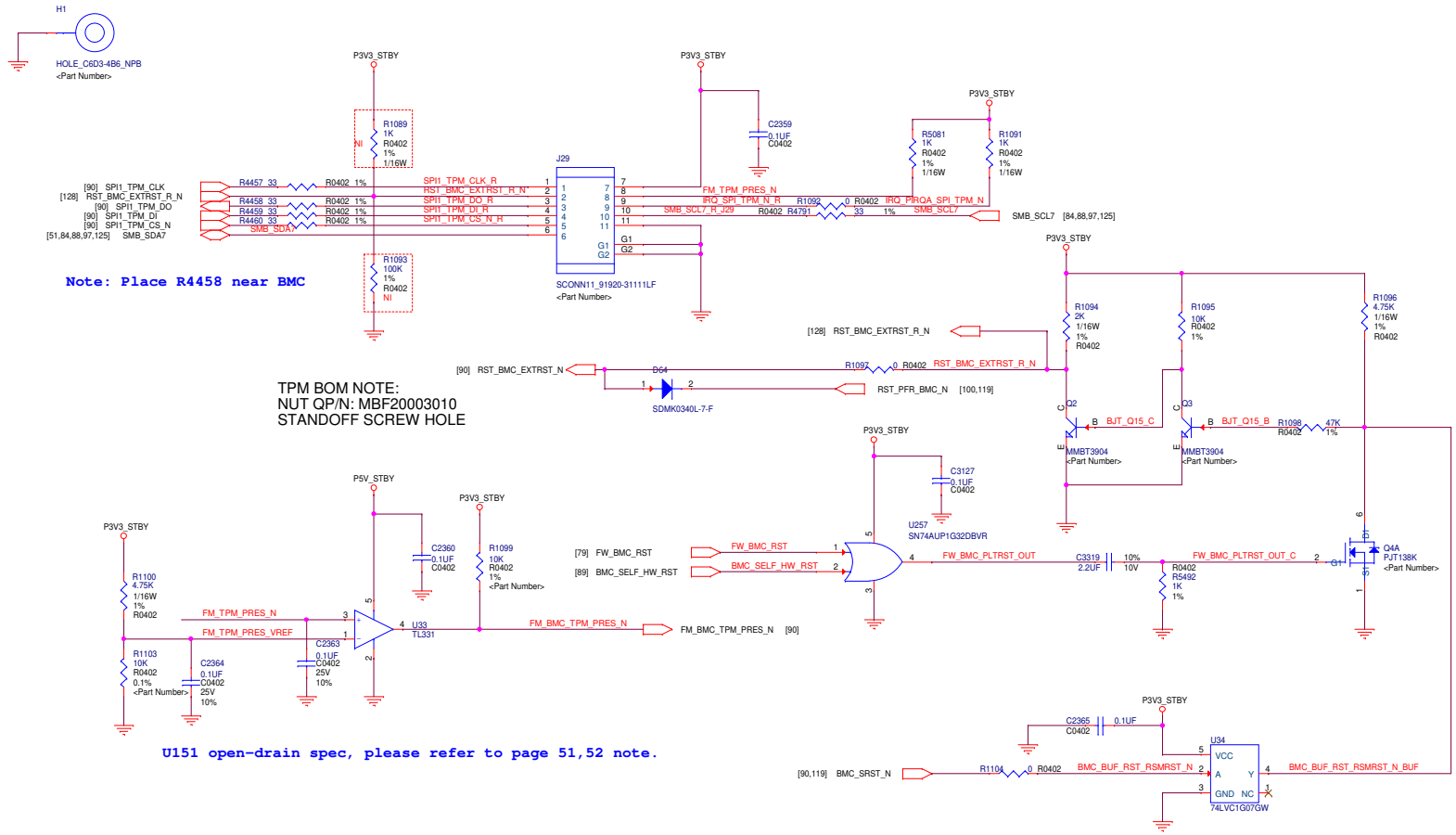
FUNCTION TABLE

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

LOGIC DIAGRAM (POSITIVE LOGIC)

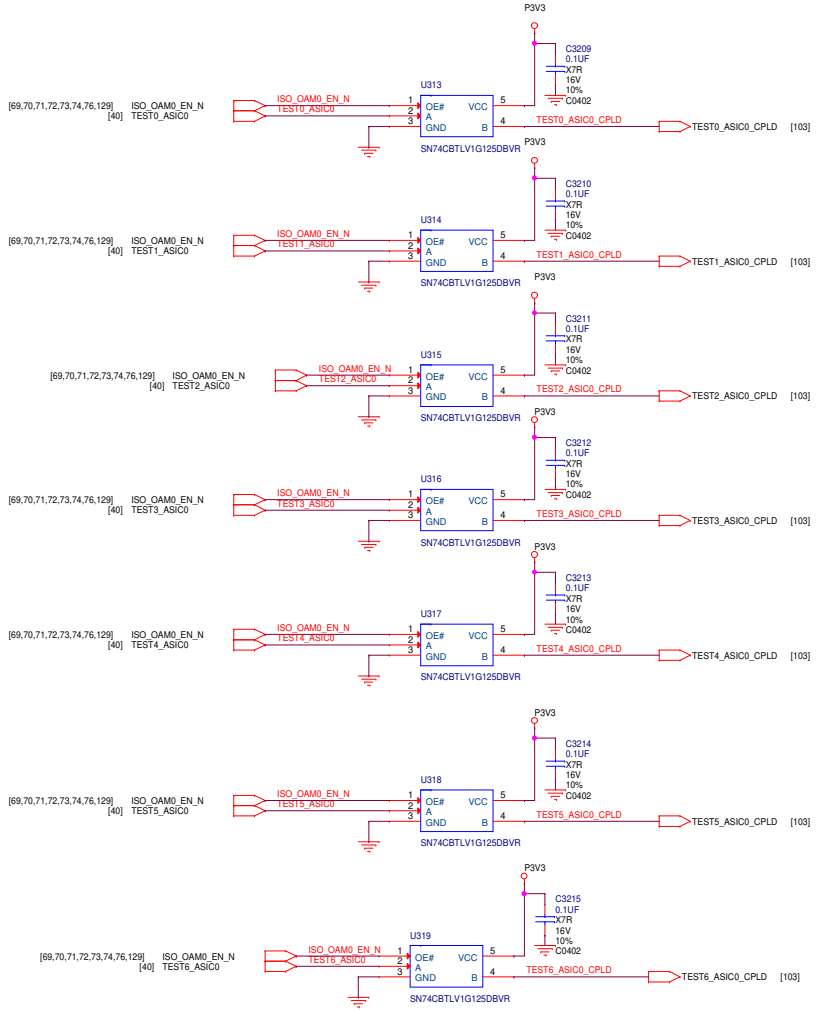


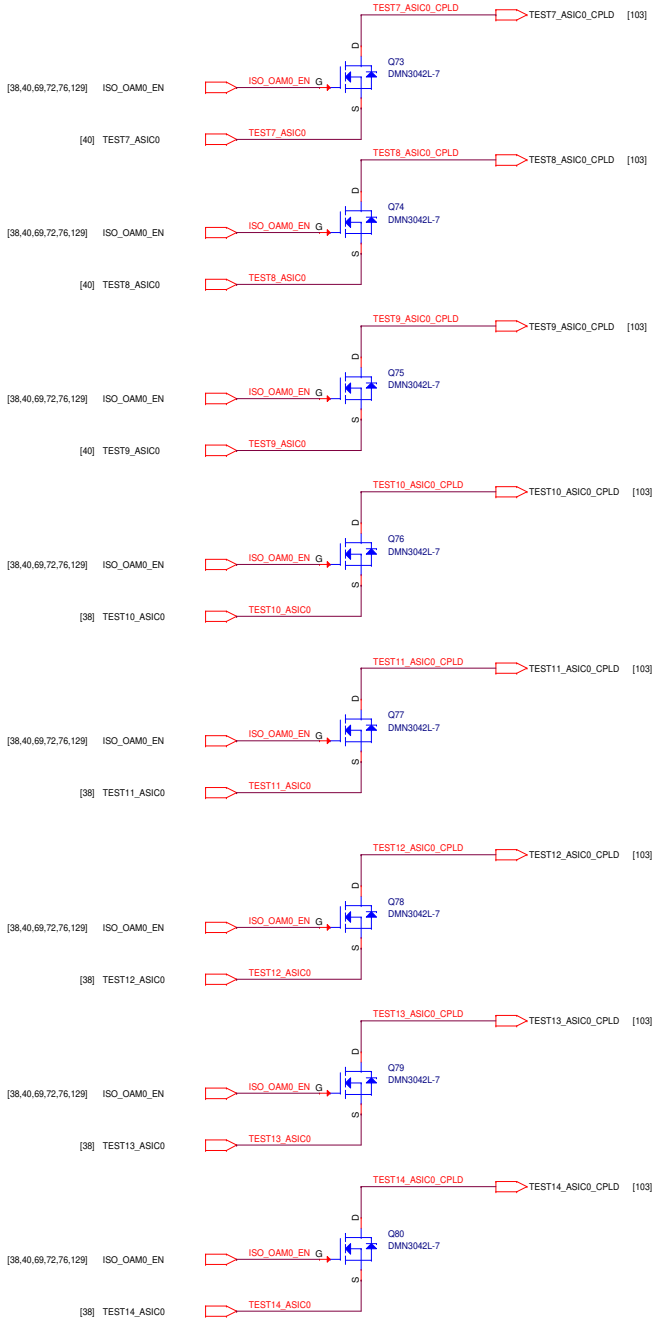
SYSTEM STATUS LED CIRIUIT



TPM CONN

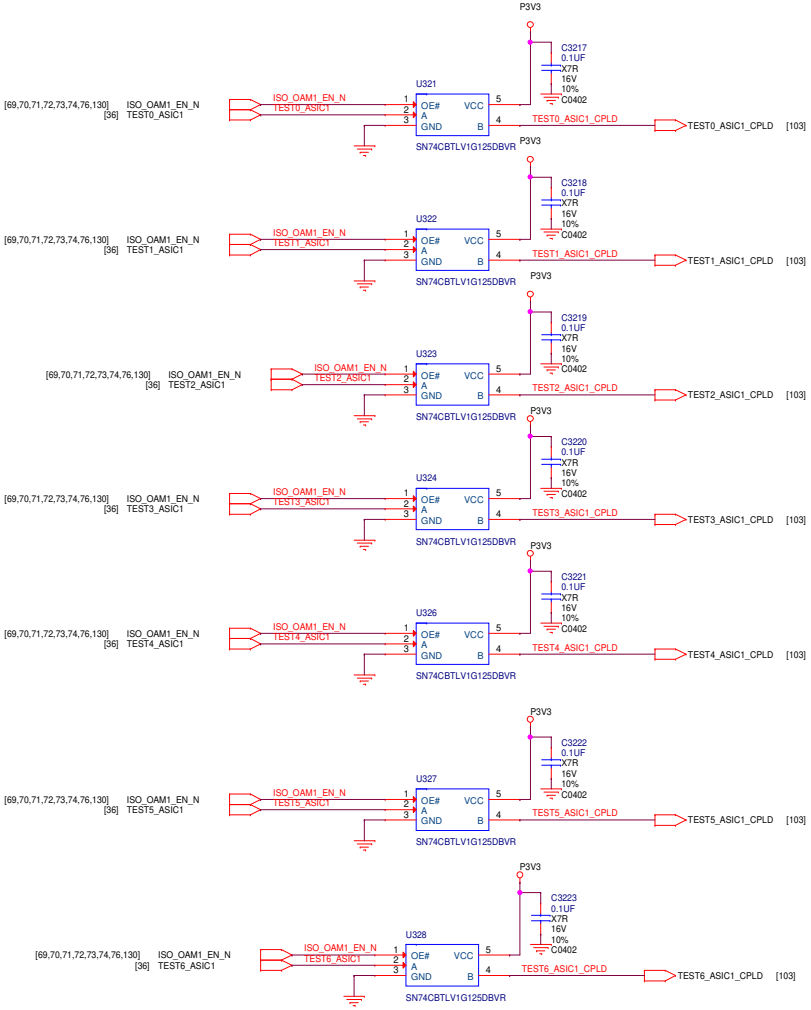
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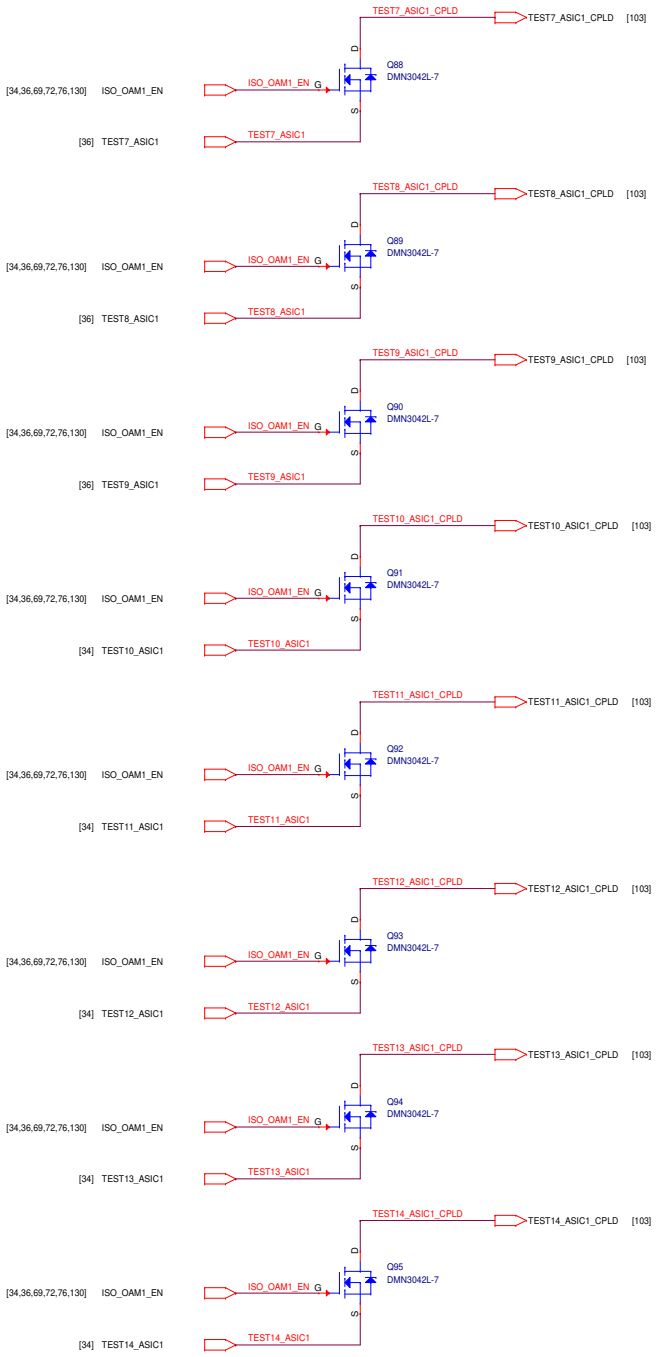




ISOLATOIN_TEST_ASIC0

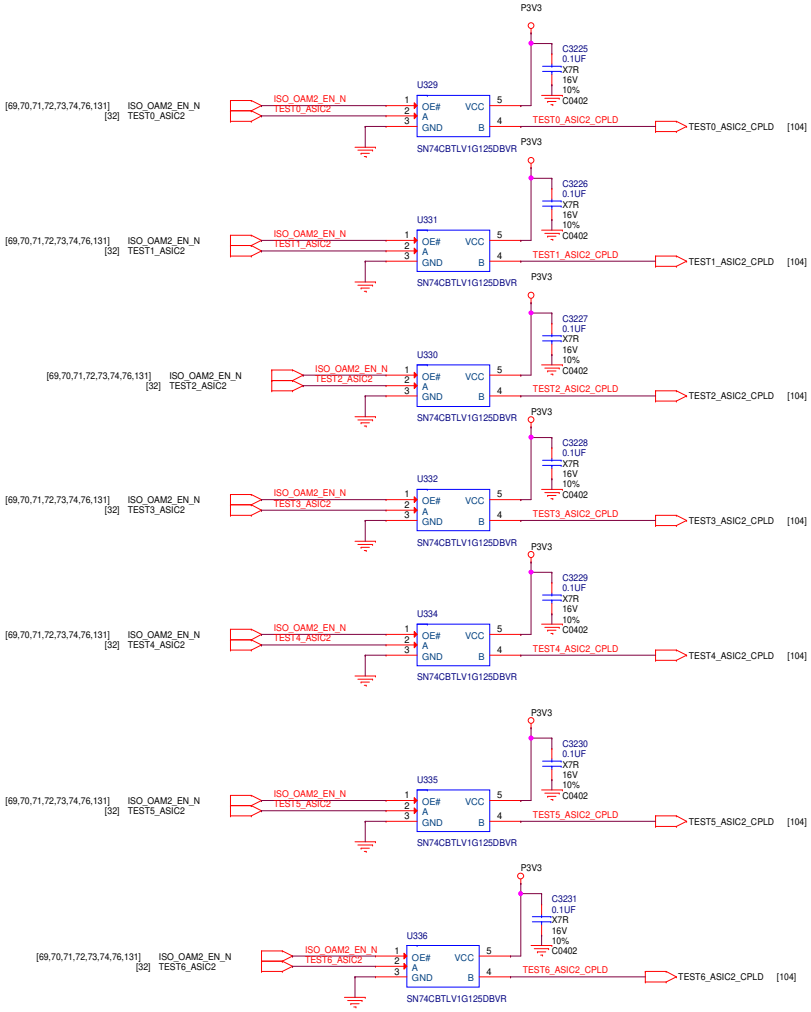
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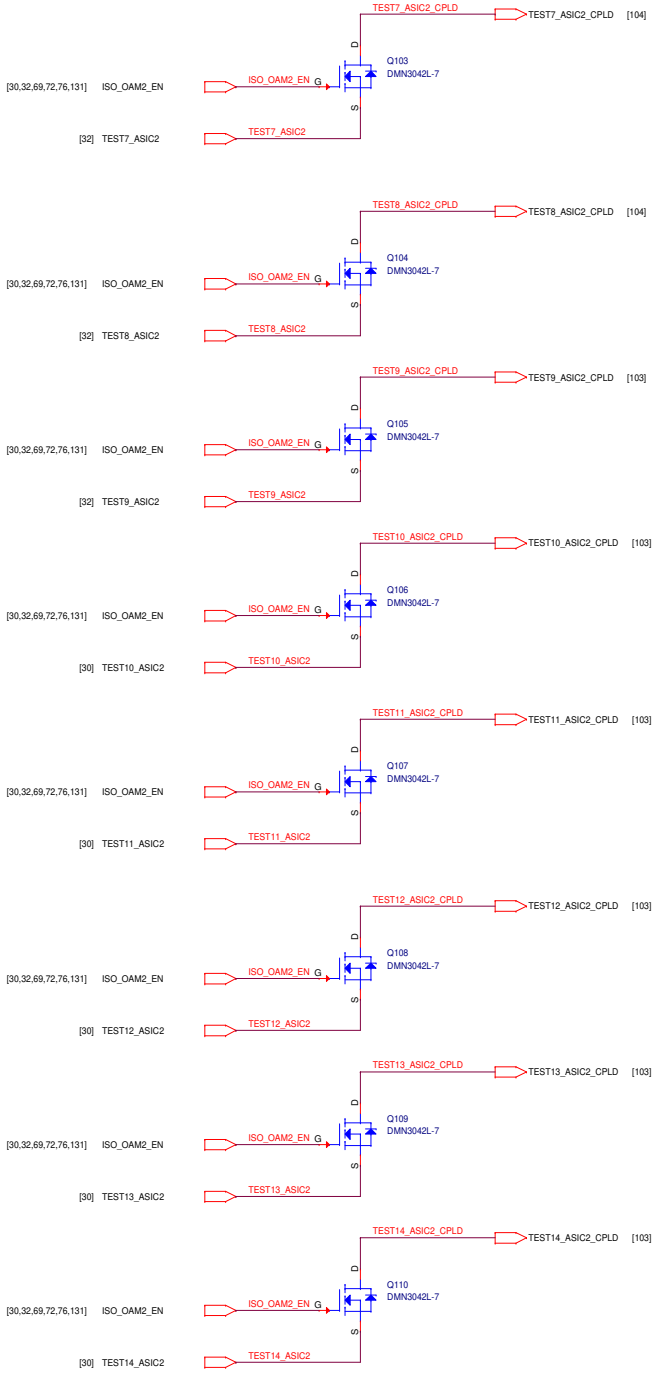




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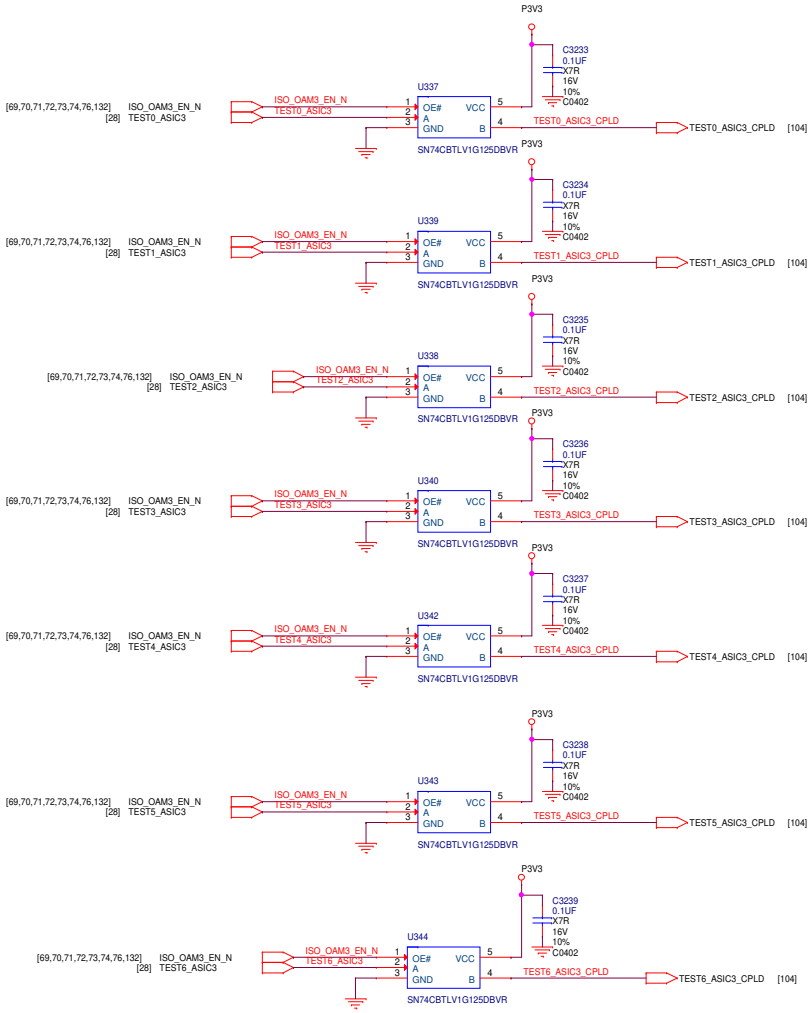
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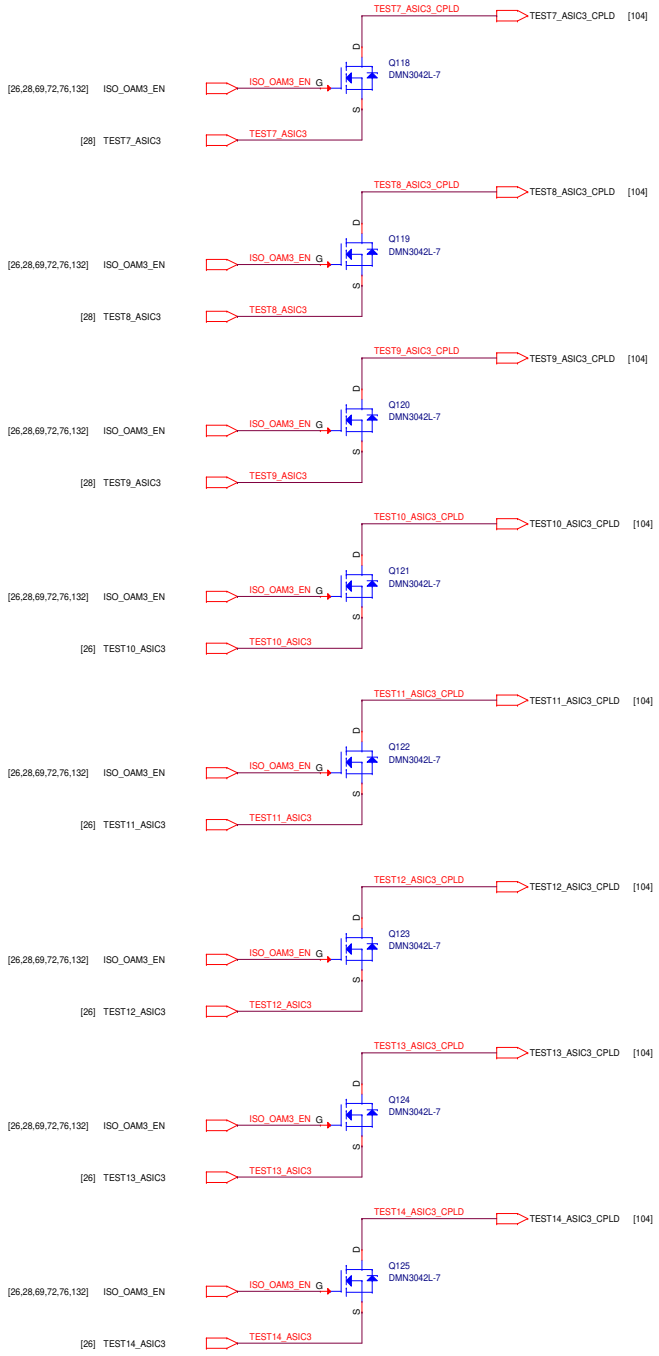




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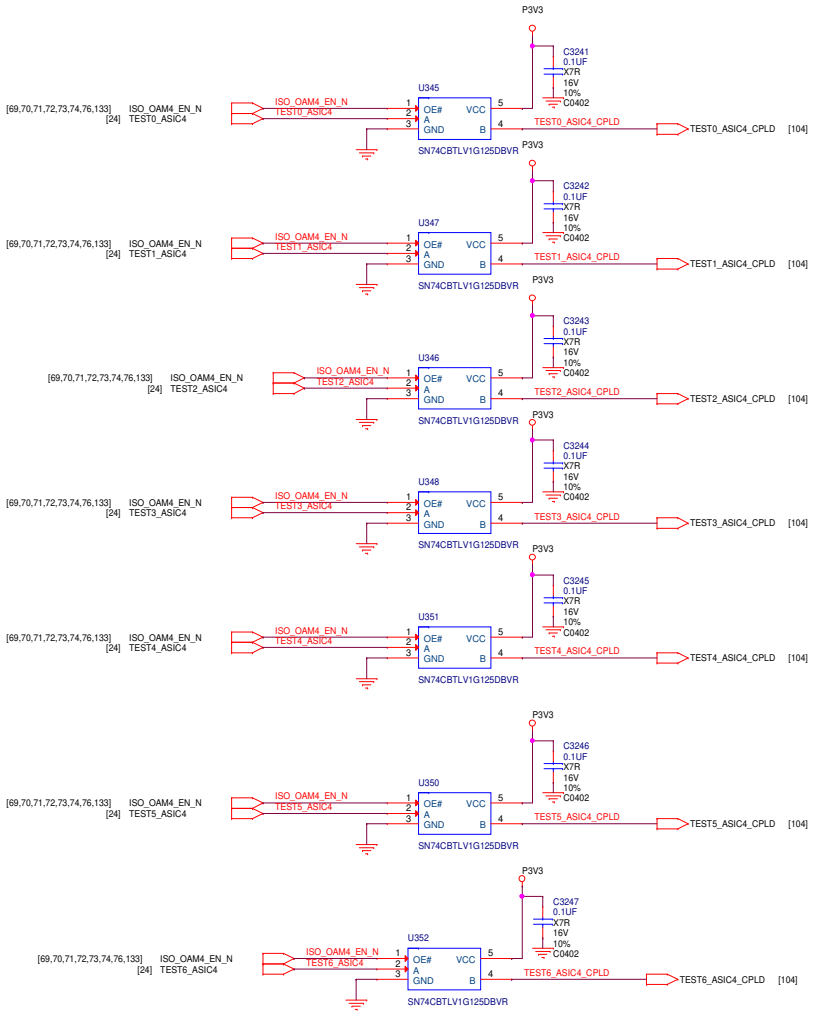
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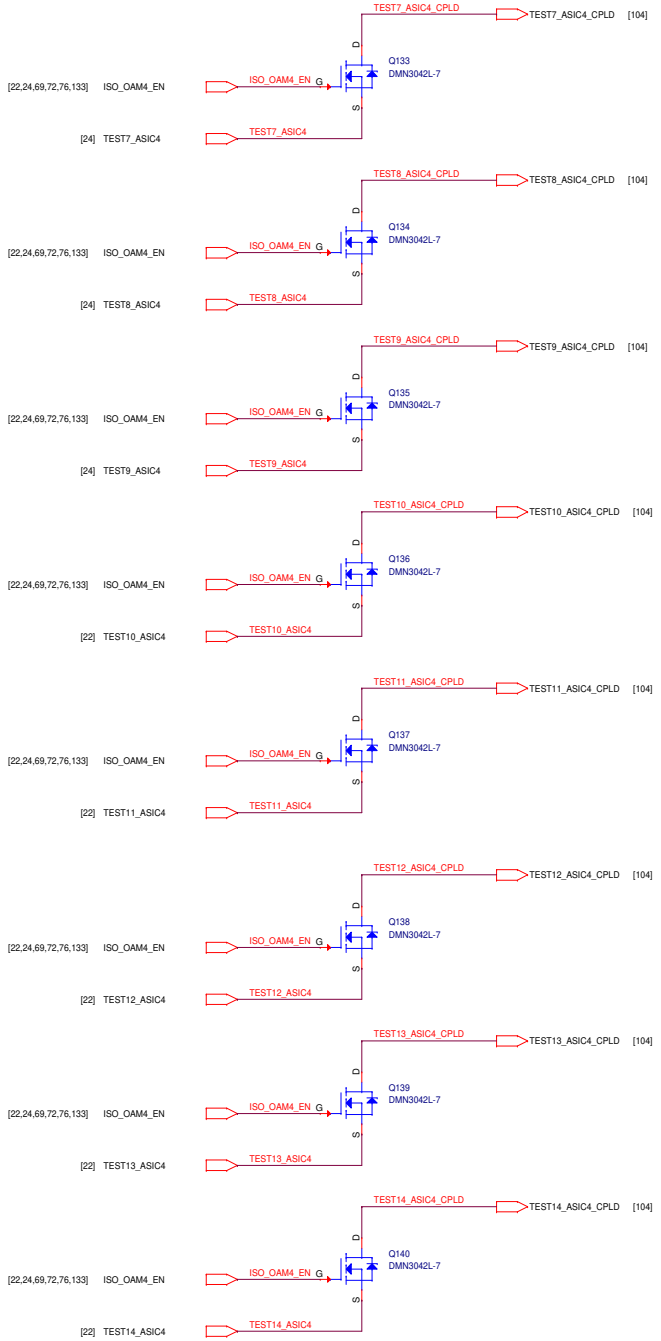




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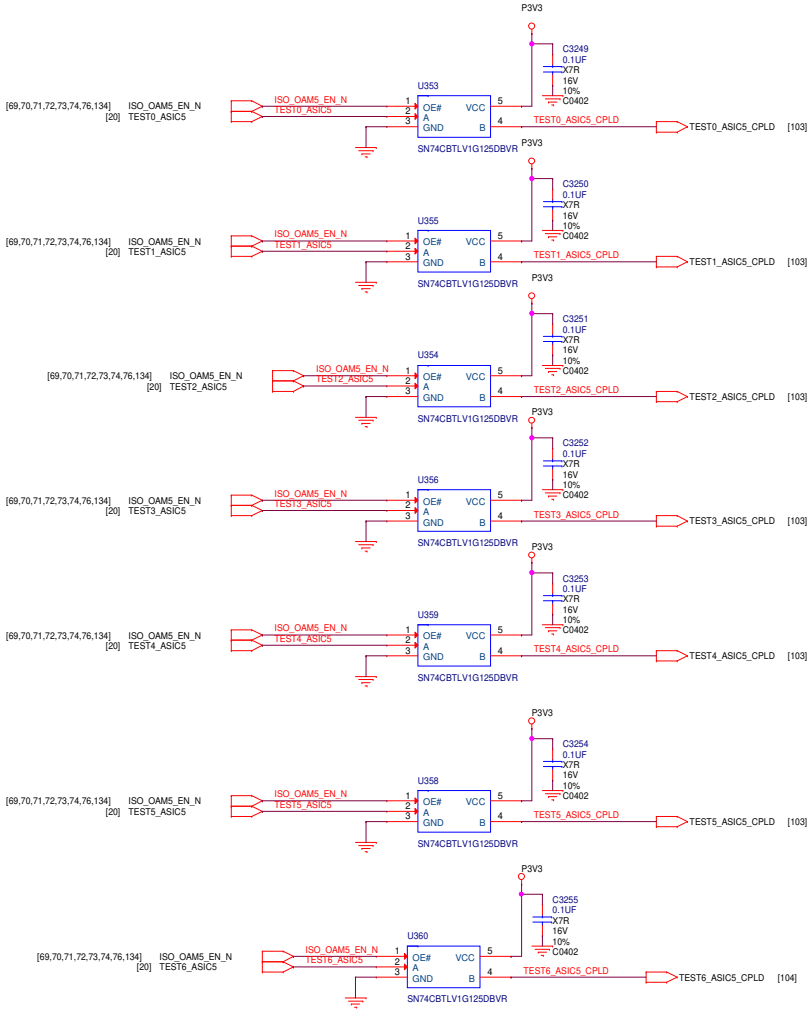
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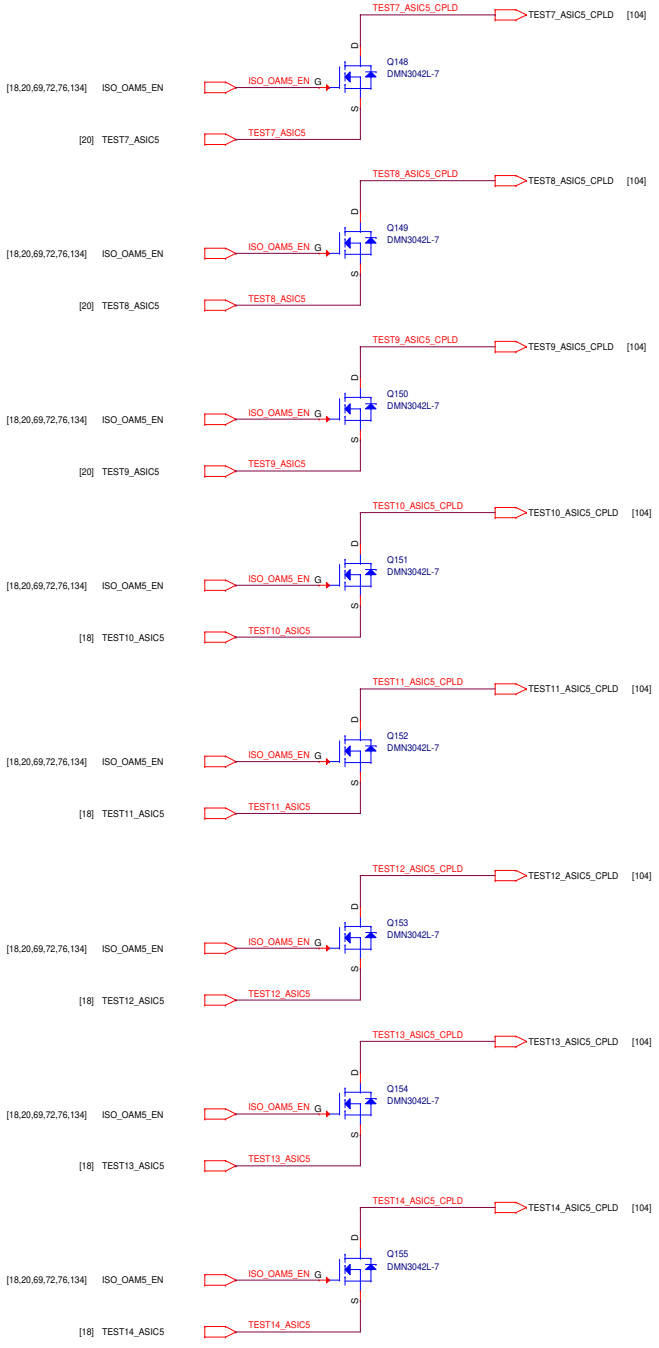




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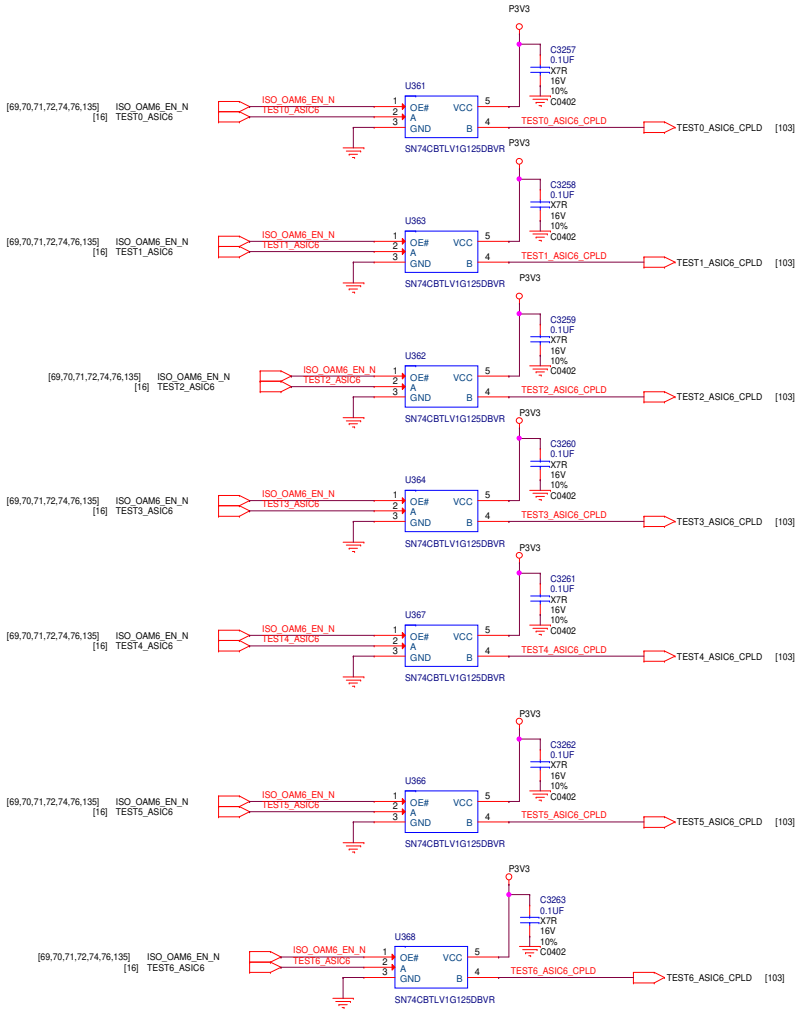
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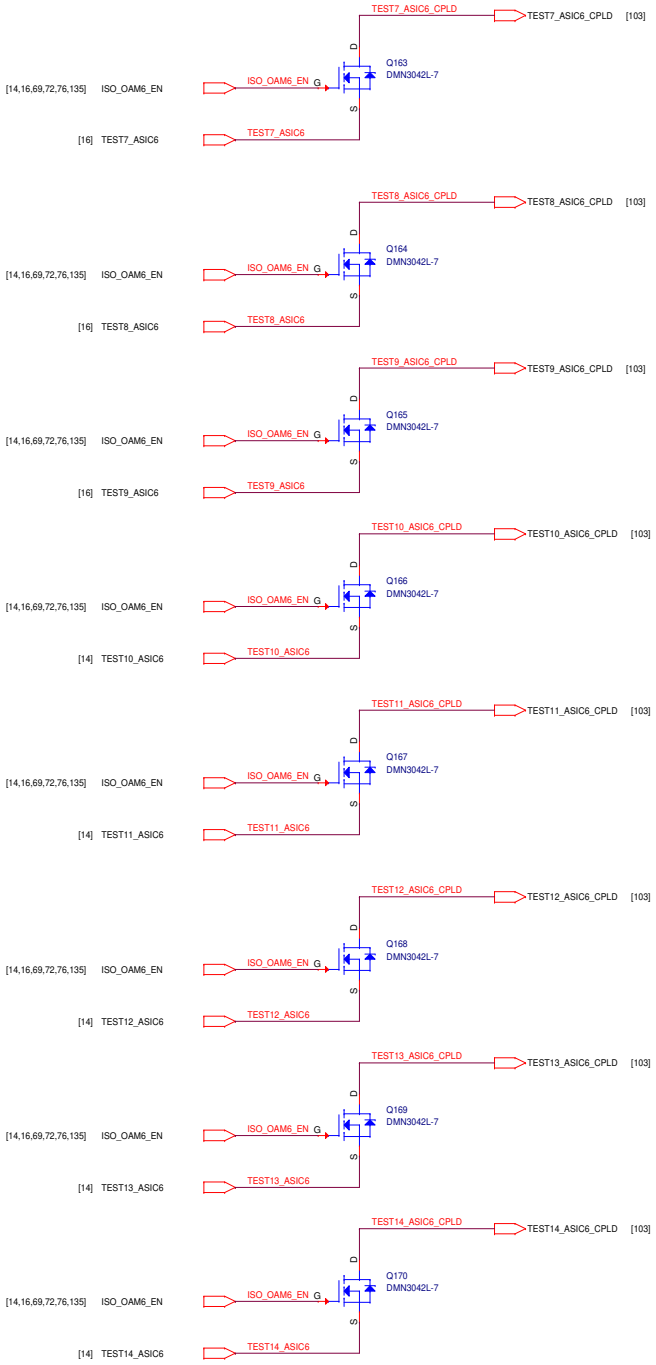




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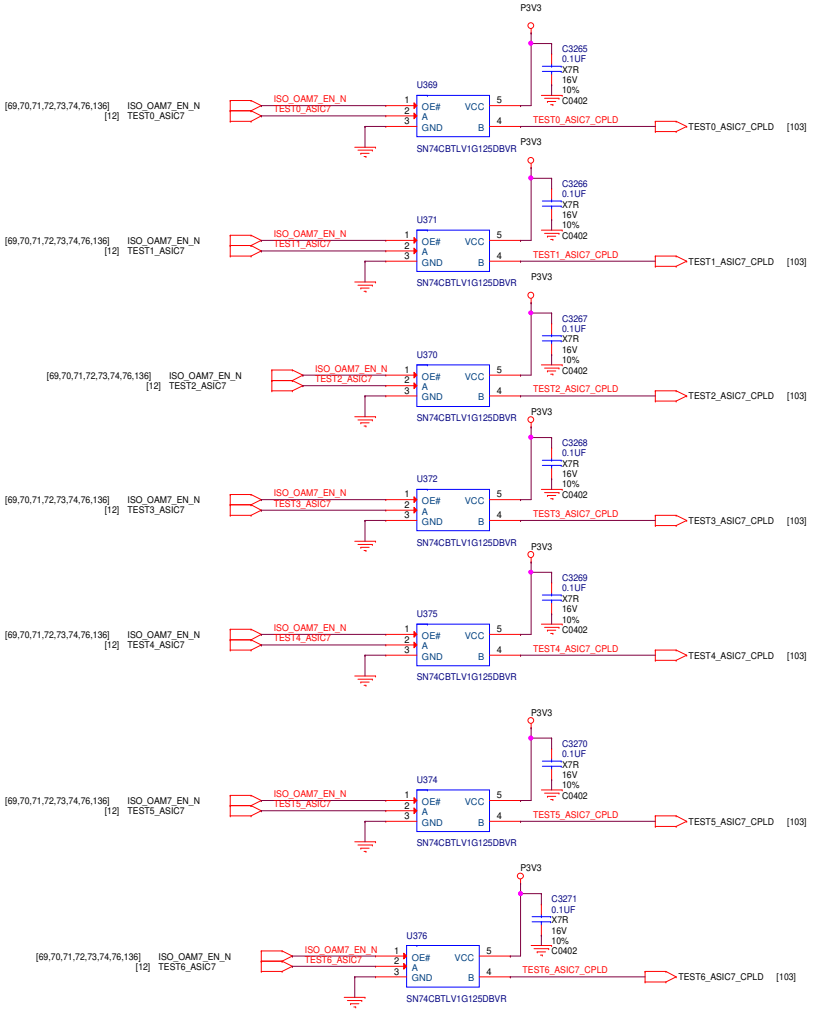
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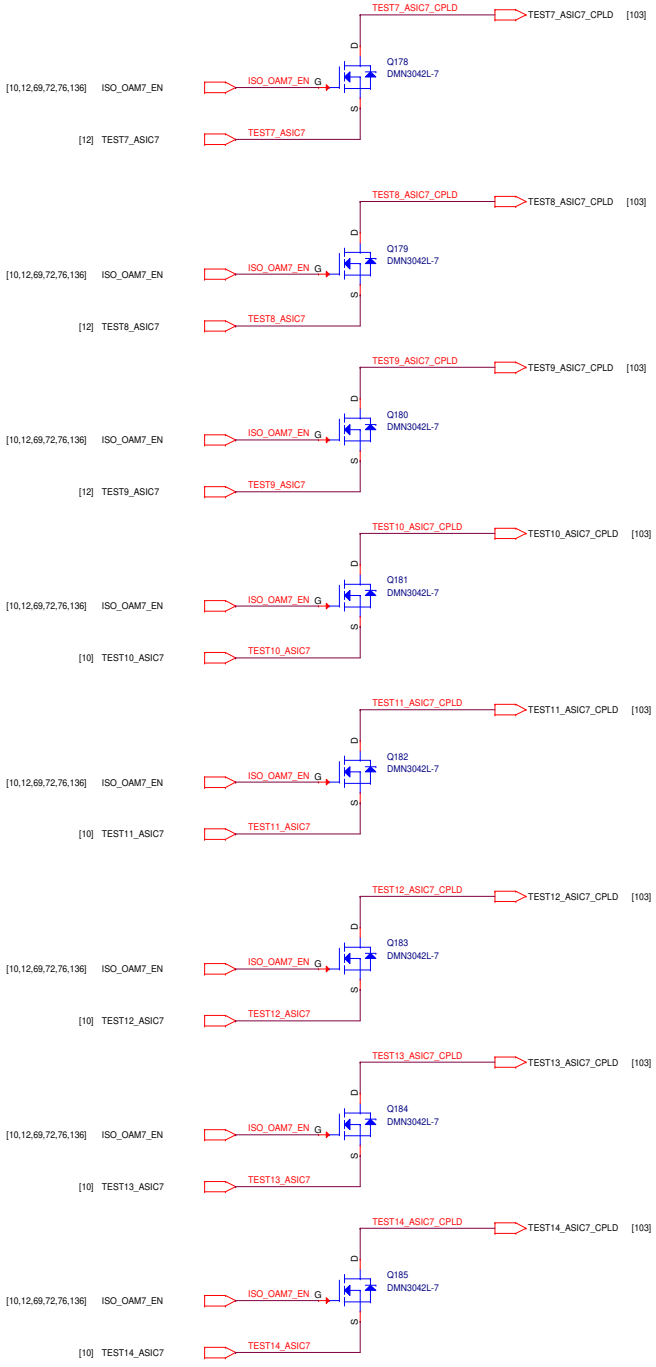




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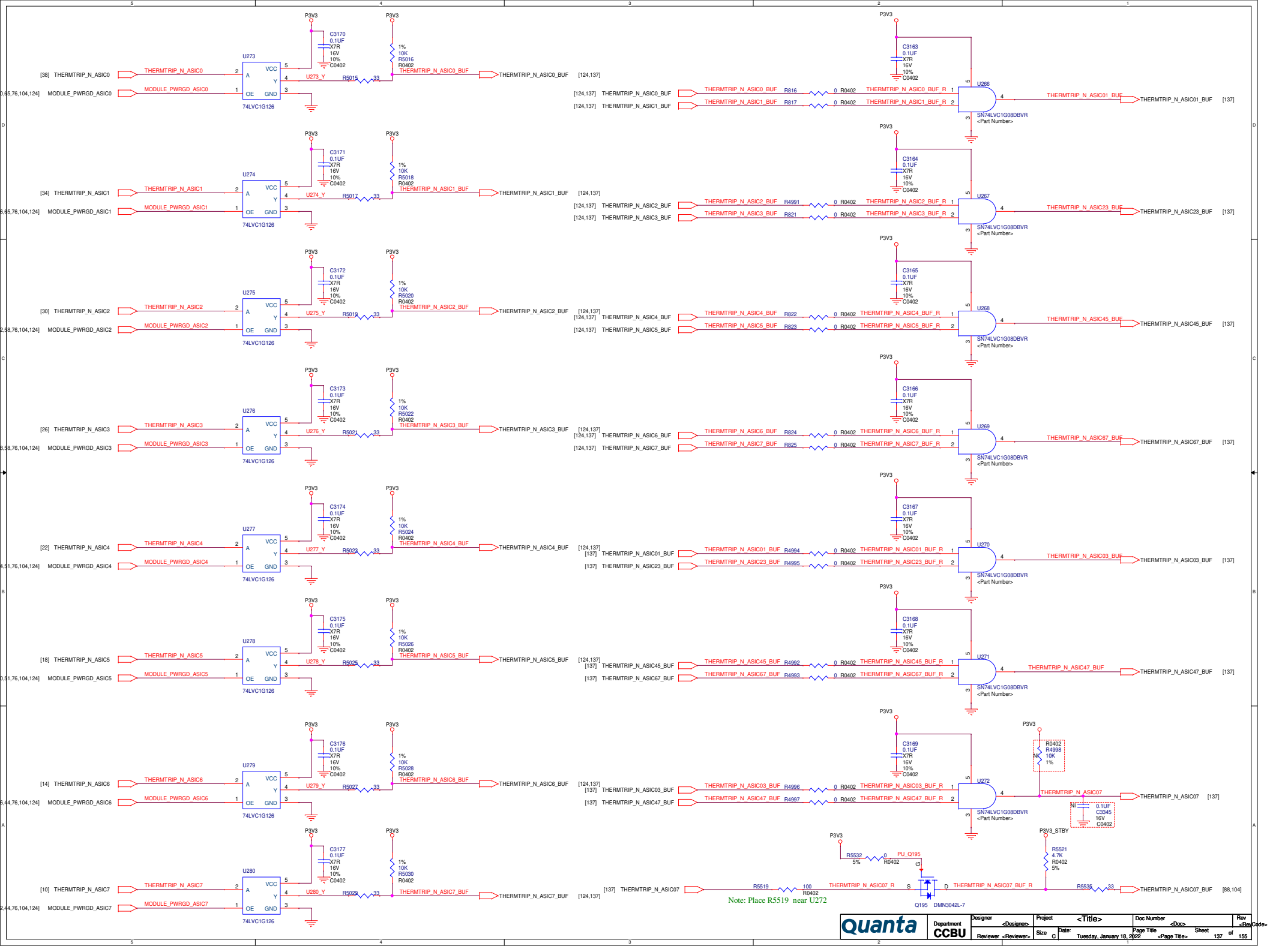
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ISOLATOIN_TEST_ASIC7

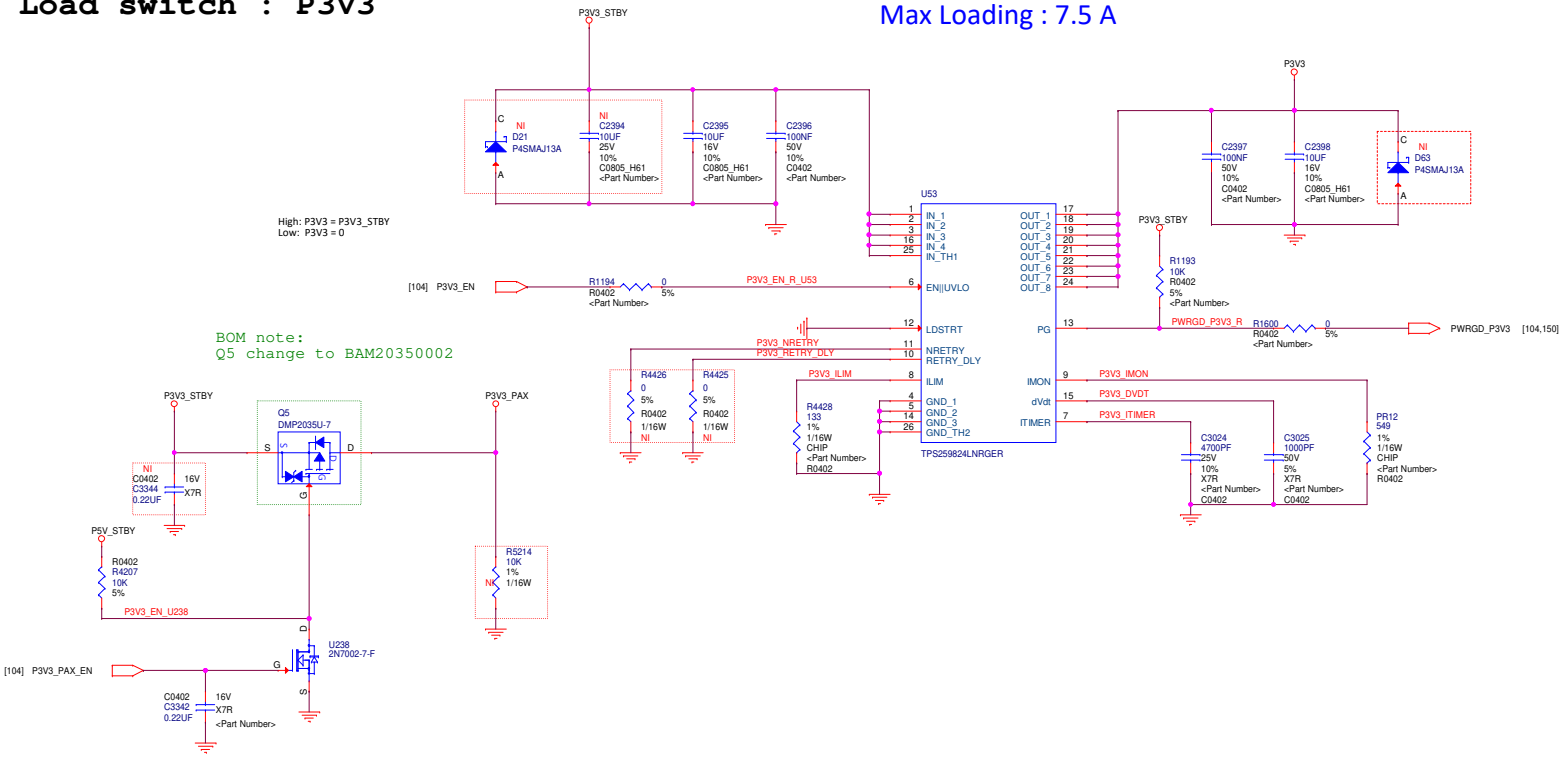
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Load switch : P3V3

Design Note
Max Loading : 7.5 A



P3V3/P5V POWER SWITCH

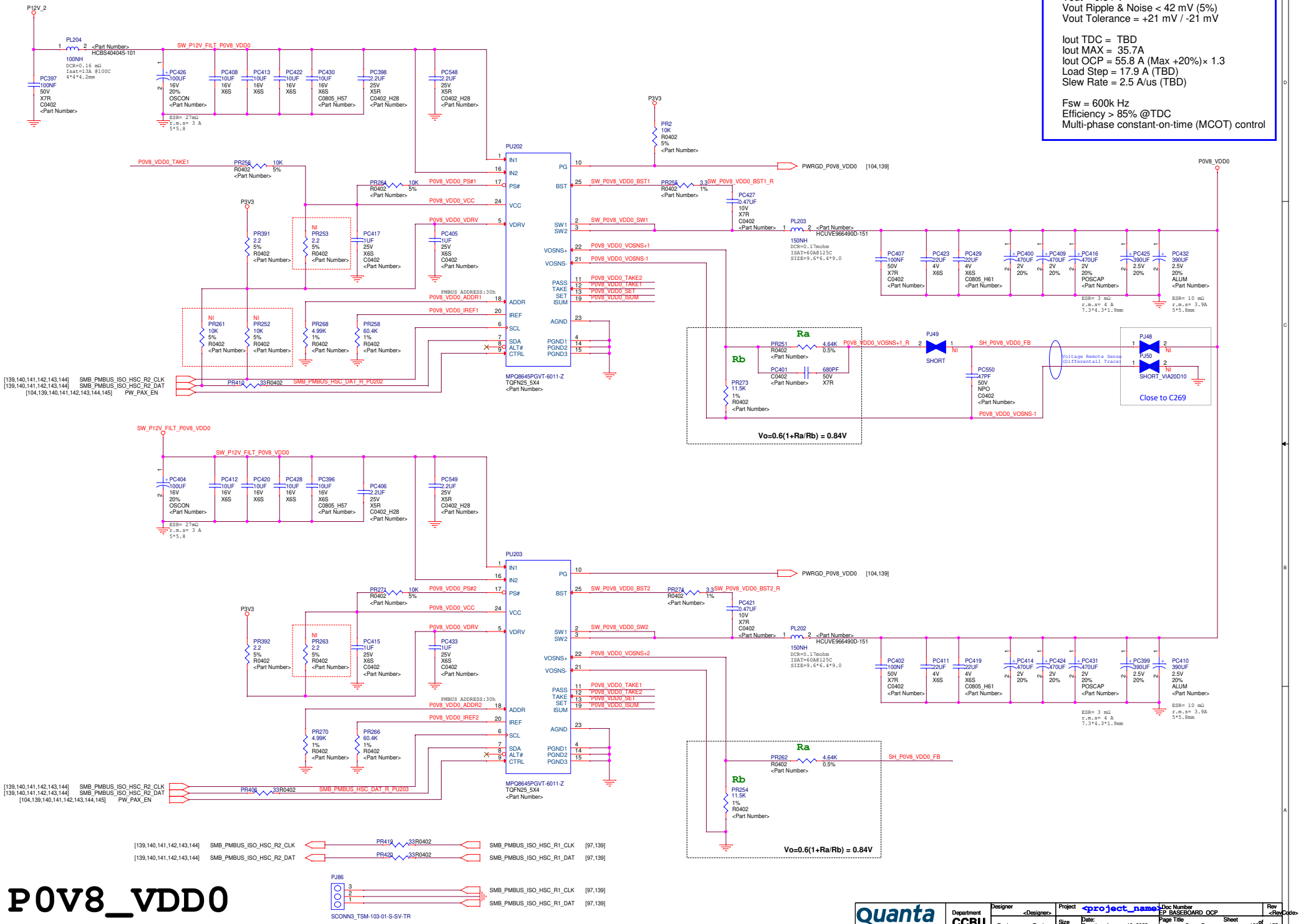
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Design specification

Vout = 0.84 V
Vout Ripple & Noise < 42 mV (5%)
Vout Tolerance = +21 mV / -21 mV

Iout TDC = TBD
Iout MAX = 35.7A
Iout OCP = 55.8 A (Max +20%)× 1.3
Load Step = 17.9 A (TBD)
Slew Rate = 2.5 A/us (TBD)

Fsw = 600k Hz
Efficiency > 85% @TDC
Multi-phase constant-on-time (MCOT) control



P0V8_VDD0

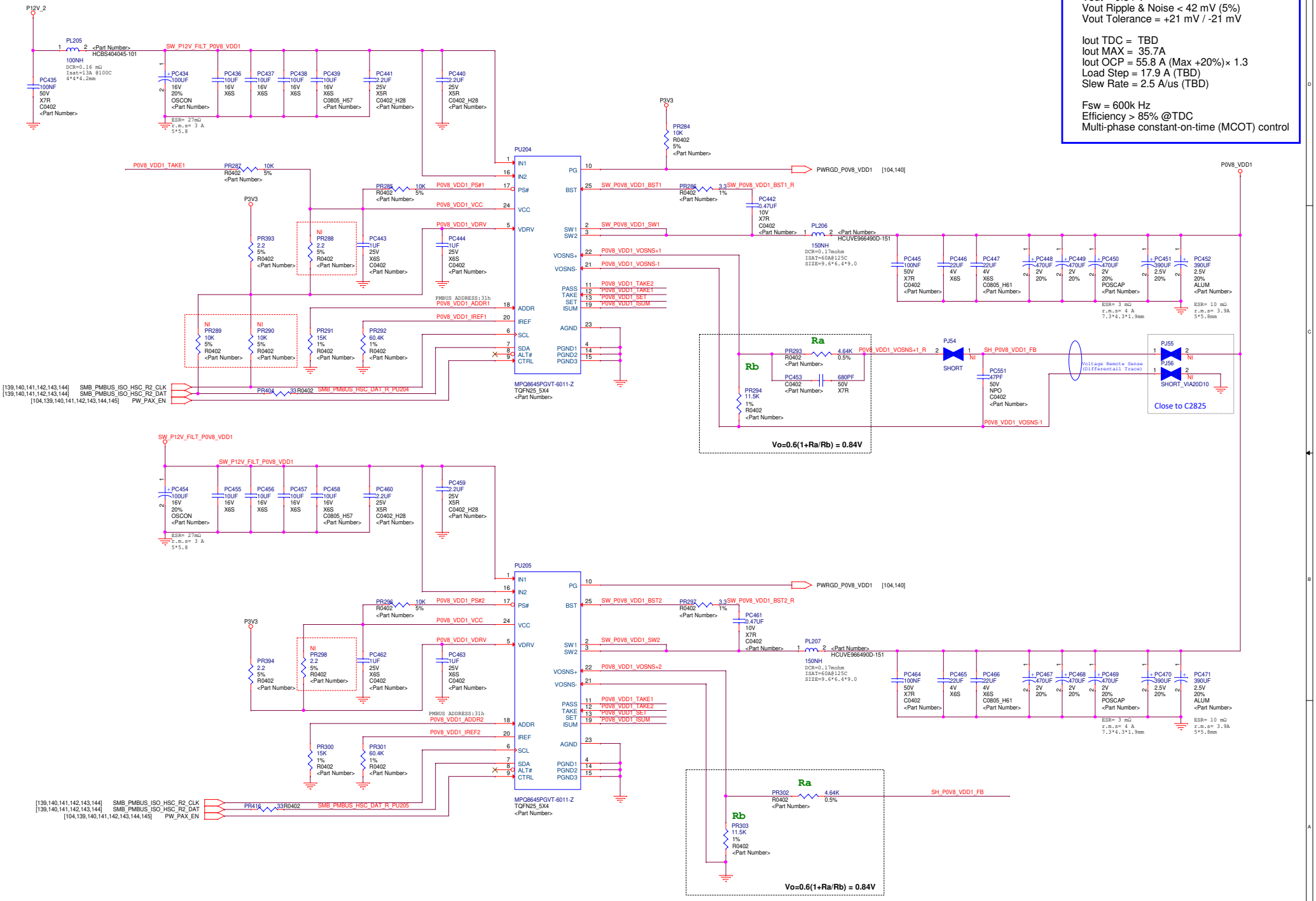
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Design specification

Vout = 0.84 V
Vout Ripple & Noise < 42 mV (5%)
Vout Tolerance = +21 mV / -21 mV

Iout TDC = TBD
Iout MAX = 35.7A
Iout OCP = 55.8 A (Max +20%)× 1.3
Load Step = 17.9 A (TBD)
Slew Rate = 2.5 A/us (TBD)

Fsw = 600k Hz
Efficiency > 85% @TDC
Multi-phase constant-on-time (MCOT) control



P0V8_VDD1

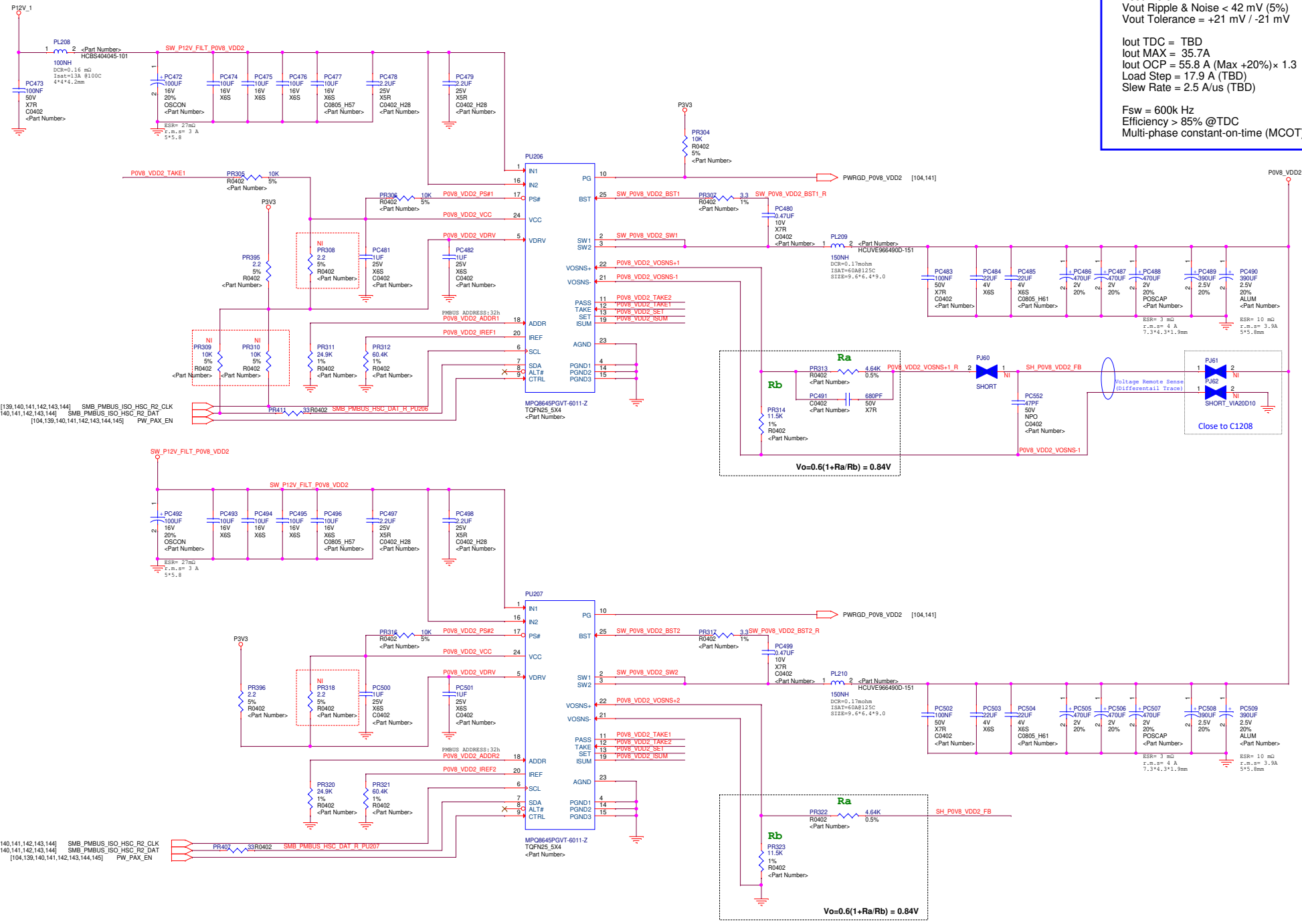
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Design specification

Vout = 0.84 V
Vout Ripple & Noise < 42 mV (5%)
Vout Tolerance = +21 mV / -21 mV

Iout TDC = TBD
Iout MAX = 35.7A
Iout OCP = 55.8 A (Max +20%)× 1.3
Load Step = 17.9 A (TBD)
Slew Rate = 2.5 A/us (TBD)

Fsw = 600k Hz
Efficiency > 85% @TDC
Multi-phase constant-on-time (MCOT) control



P0V8_VDD2

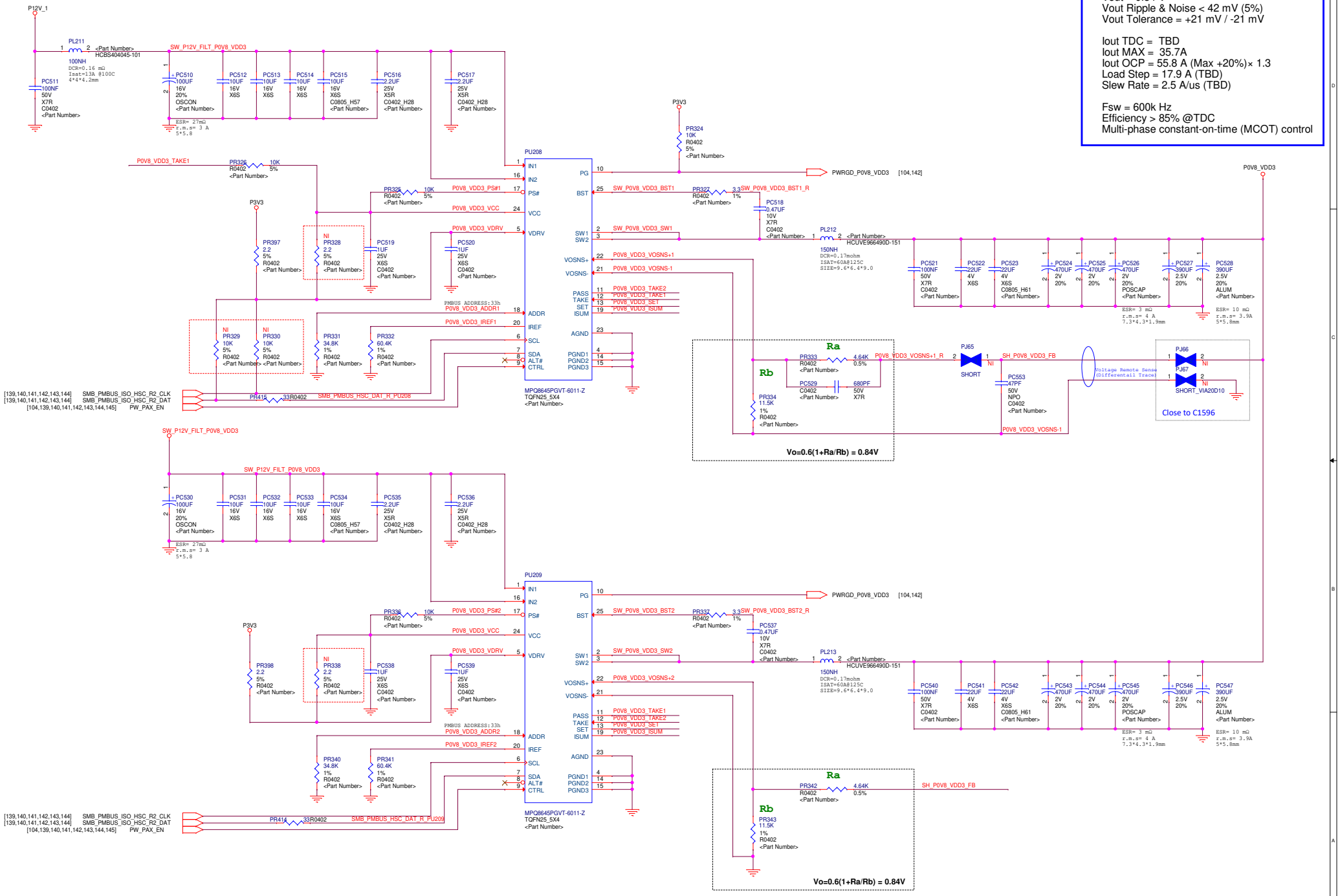
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Design specification

Vout = 0.84 V
Vout Ripple & Noise < 42 mV (5%)
Vout Tolerance = +21 mV / -21 mV

Iout TDC = TBD
Iout MAX = 35.7A
Iout OCP = 55.8 A (Max +20%)× 1.3
Load Step = 17.9 A (TBD)
Slew Rate = 2.5 A/us (TBD)

Fsw = 600k Hz
Efficiency > 85% @TDC
Multi-phase constant-on-time (MCOT) control



P0V8_VDD3

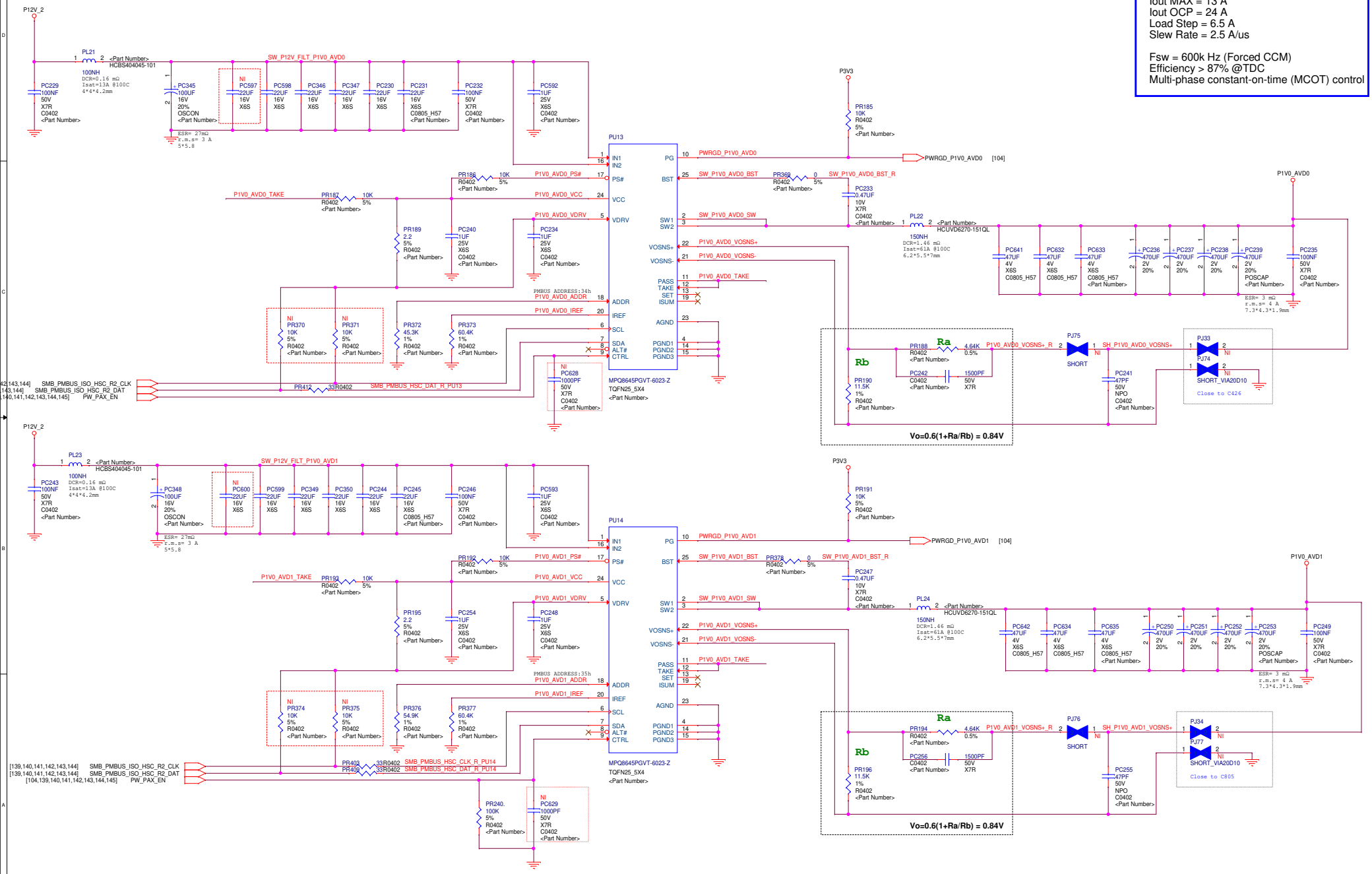
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Design specification

Vout = 0.84 V
Vout Ripple & Noise < 42 mV (5%)
Vout Tolerance = +21 mV / -21 mV

Iout TDC = 10.29 A
Iout MAX = 13 A
Iout OCP = 24 A
Load Step = 6.5 A
Slew Rate = 2.5 A/us

Fsw = 600k Hz (Forced CCM)
Efficiency > 87% @TDC
Multi-phase constant-on-time (MCOT) control



P1V0_AVD0/1

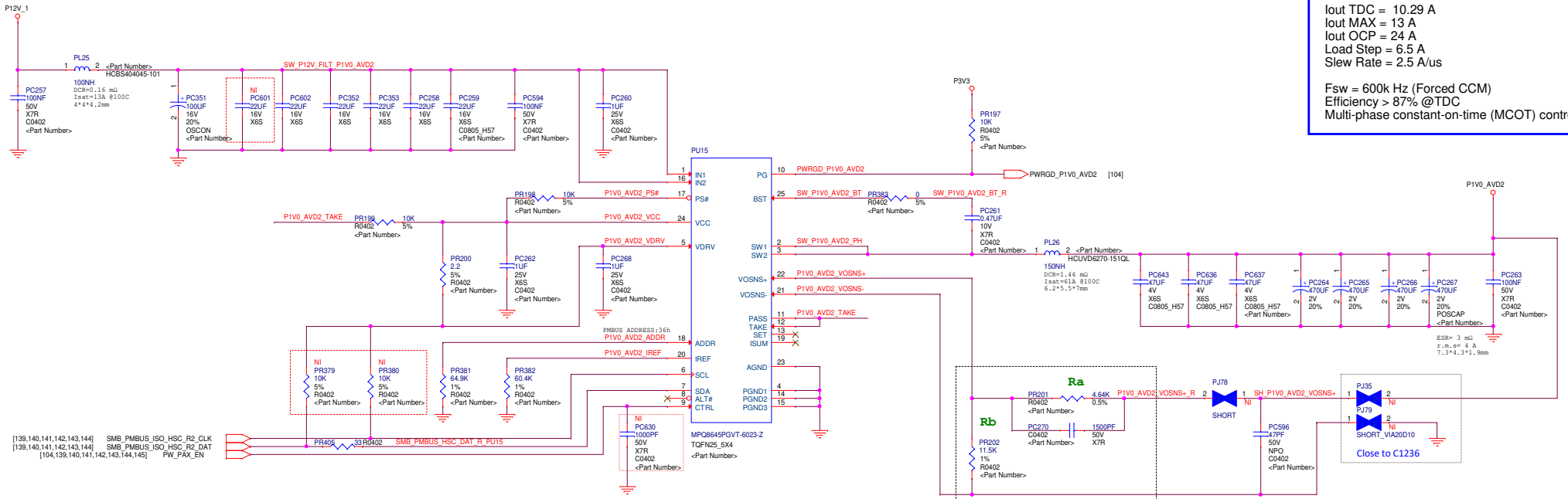
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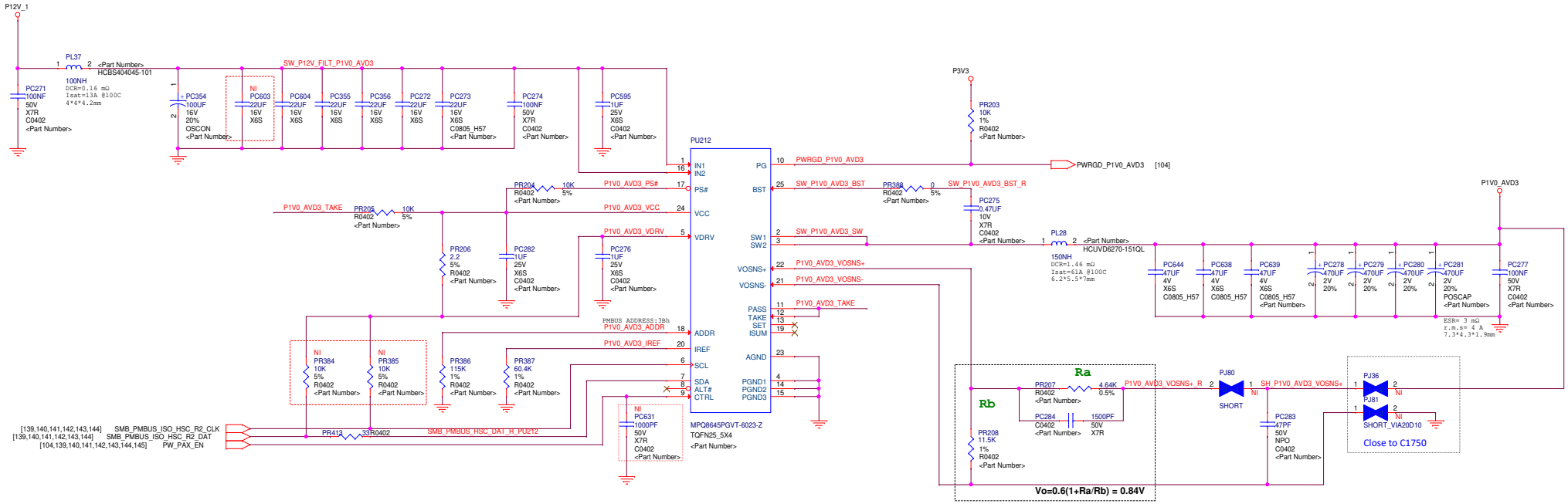
Design specification

Vout = 0.84 V
Vout Ripple & Noise < 42 mV (5%)
Vout Tolerance = +21 mV / -21 mV

Iout TDC = 10.29 A
Iout MAX = 13 A
Iout OCP = 24 A
Load Step = 6.5 A
Slew Rate = 2.5 A/us

Fsw = 600k Hz (Forced CCM)
Efficiency > 87% @TDC
Multi-phase constant-on-time (MCOT) control





P1V0_AVD2/3

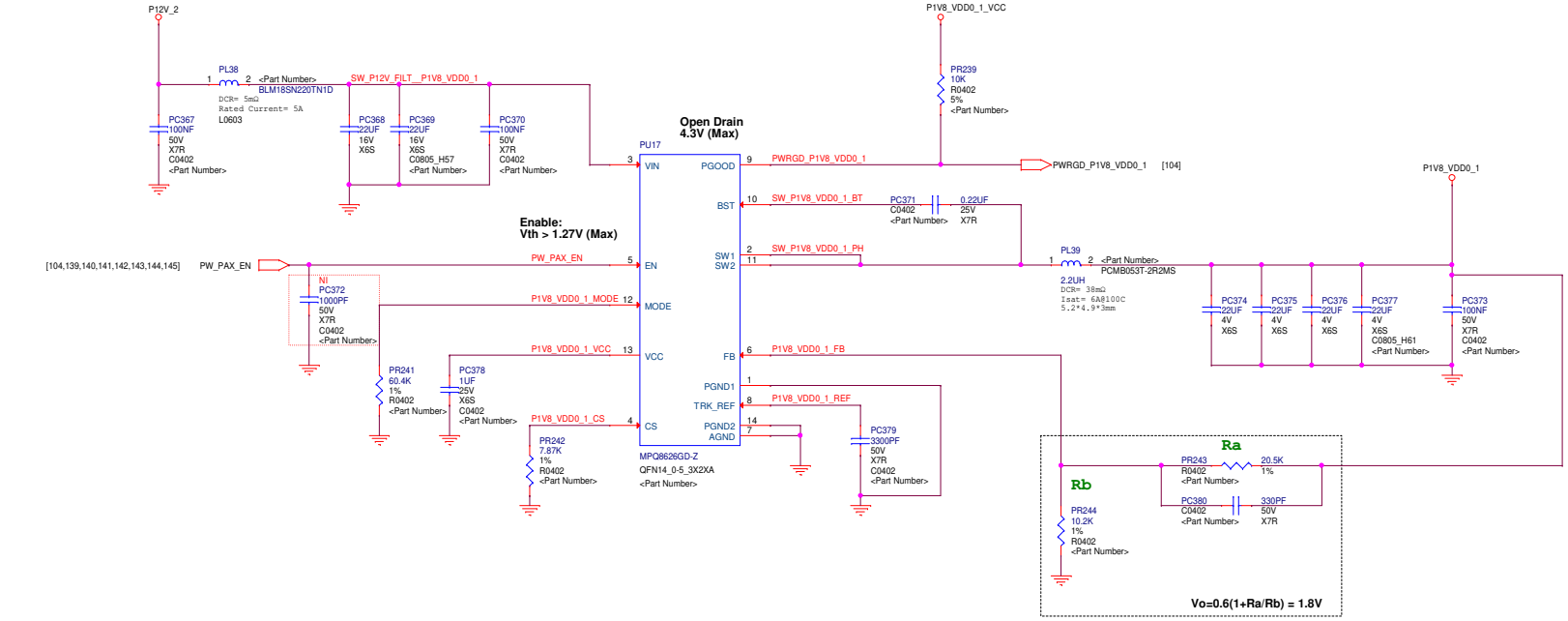
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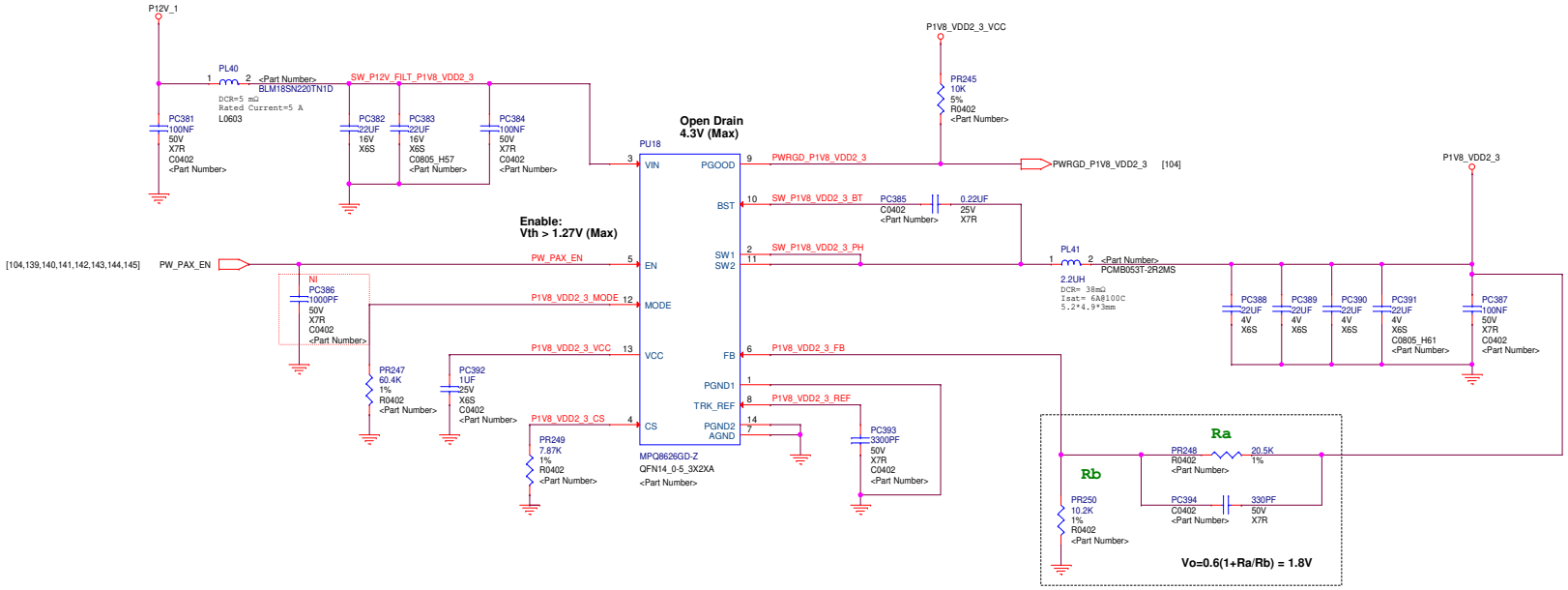
Design specification

Vout = 1.8 V
Vout Ripple & Noise < 90 mV (5%)
Vout Tolerance = +45 mV / -45 mV

Iout TDC = TBD
Iout MAX = 3.96 A
Iout OCP = 4.4A
Load Step = 1.2 A (TBD)
Slew Rate = 2.5 A/us (TBD)

Fsw = 600k Hz (Forced CCM)
Efficiency > 85% @TDC
COT Control Mode





P1V8_VDD0/1/2/3

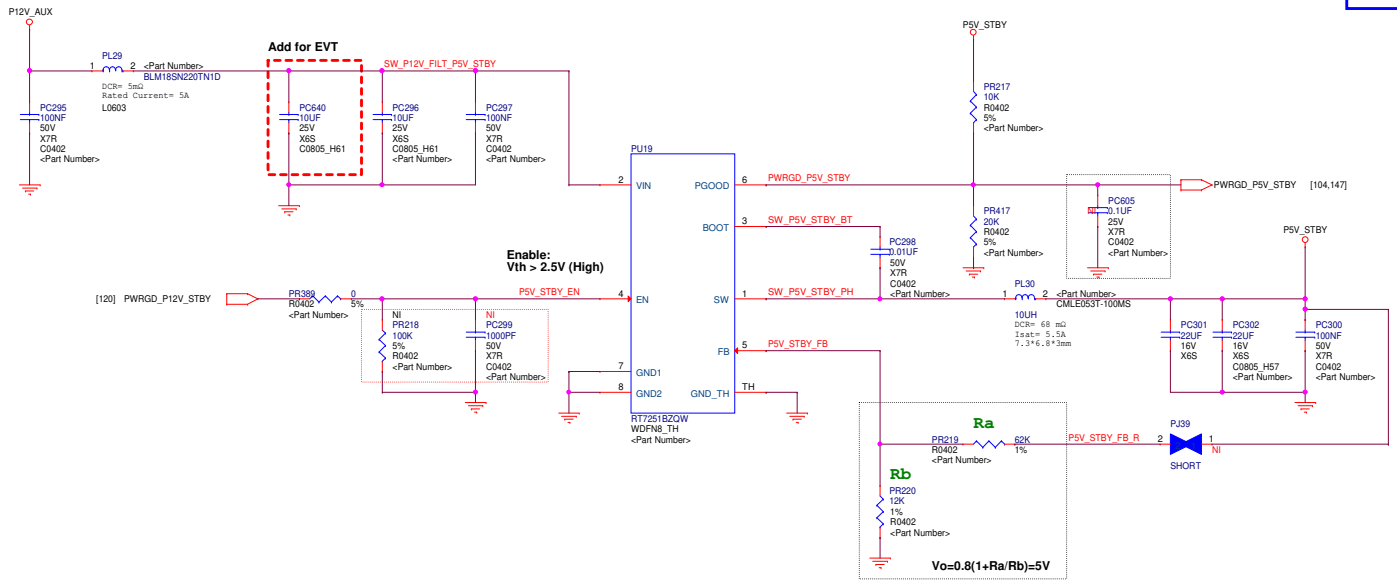
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Design specification

Vout = 5V
Vout Ripple & Noise < 50mV (1%)
Vout Tolerance = +250 mV / -250 mV

Iout TDC = (TBD)
Iout MAX = 0.9 A
Iout OCP = 2.8 A (Spec)
Load Step = 0.45A (TBD)
Slew Rate = 2.5A/us (TBD)

Fsw = 800k Hz (Fixed)
Efficiency > 90% @TDC
Current Mode Control



P5V_STBY

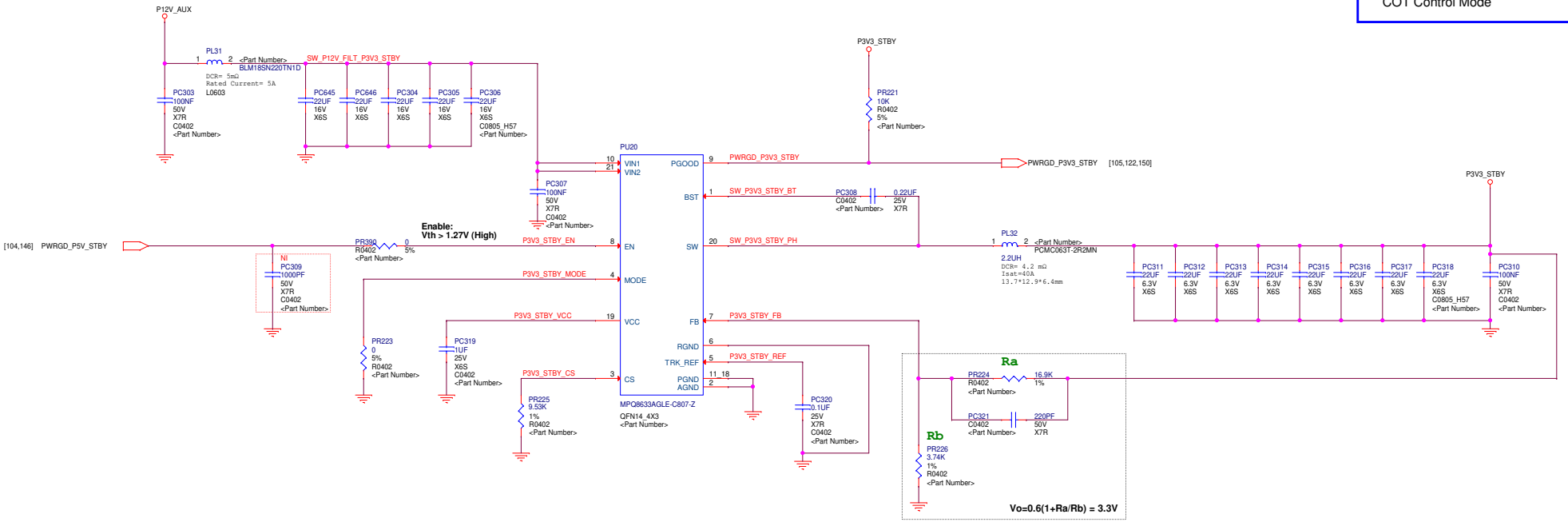
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Design specification

Vout = 3.3 V
Vout Ripple & Noise = 33 mV (1%)
Vout Tolerance = +165 mV / -165 mV(5%)

Iout TDC = TBD
Iout MAX = 5.5A
Iout OCP = 7.15 A (Max Rating × 1.3)
Load Step = 2.25A (TBD)
Slew Rate = 2.5A/us (TBD)

Fsw = 600k Hz (Forced CCM)
Efficiency > 90% @TDC
COT Control Mode



P3V3_STBY

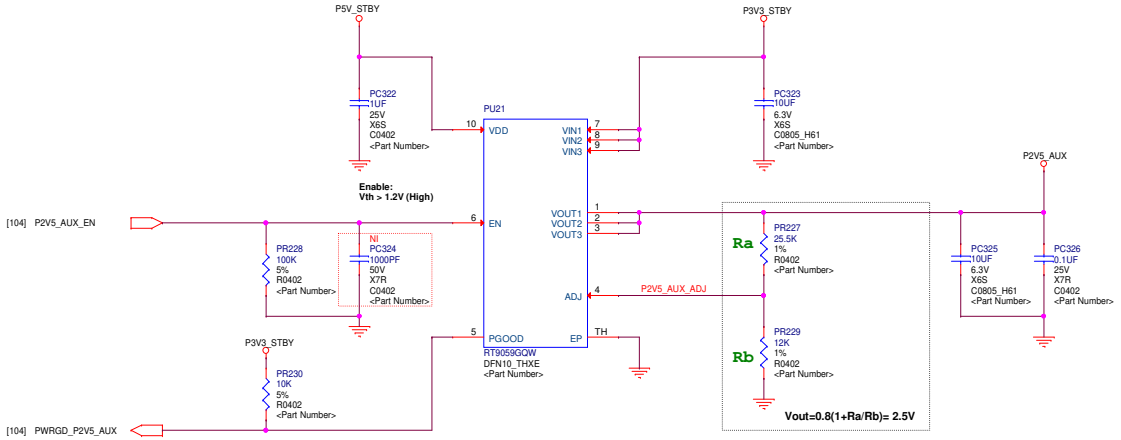
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Design specification

Vout = 2.5V
Vout Ripple & Noise < 50 mV (2%)
Vout Tolerance = +125 mV / -125 mV

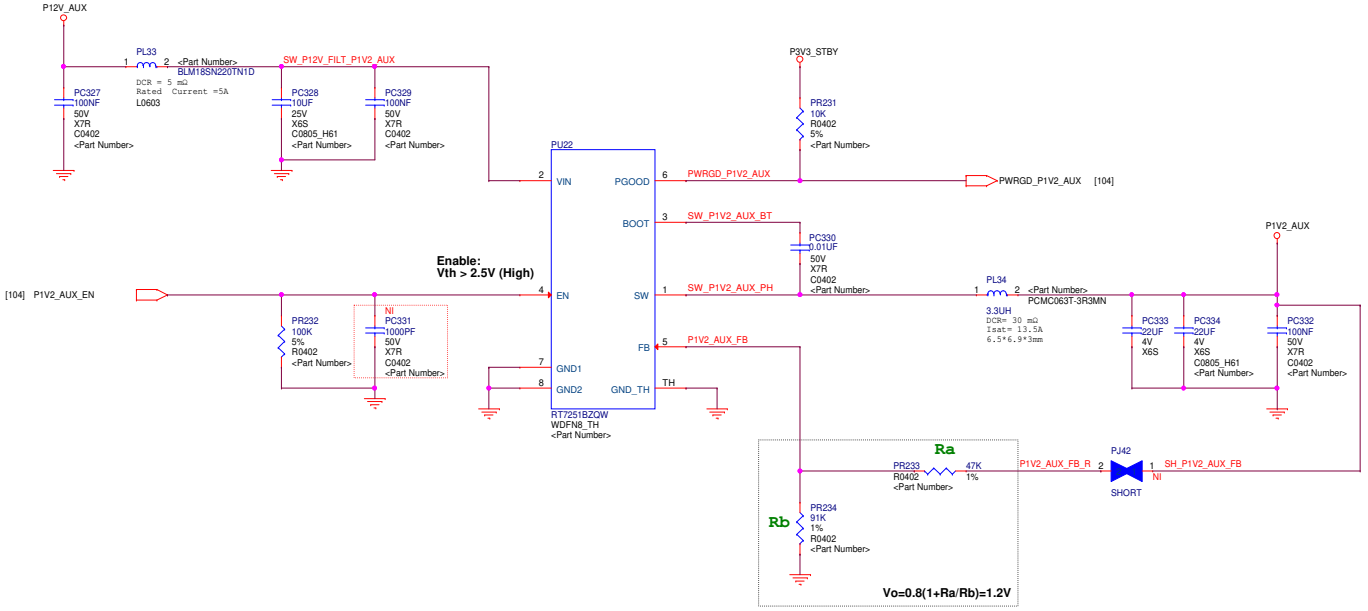
Iout MAX = 5 mA
Iout OCP = 3.6 A (Spec)
Load Step = 0.1 A (TBD)
Slew Rate = 2.5A/us (TBD)

LDO
PD=(3.3-2.5)*0.005 = 0.003W



P2V5_AUX

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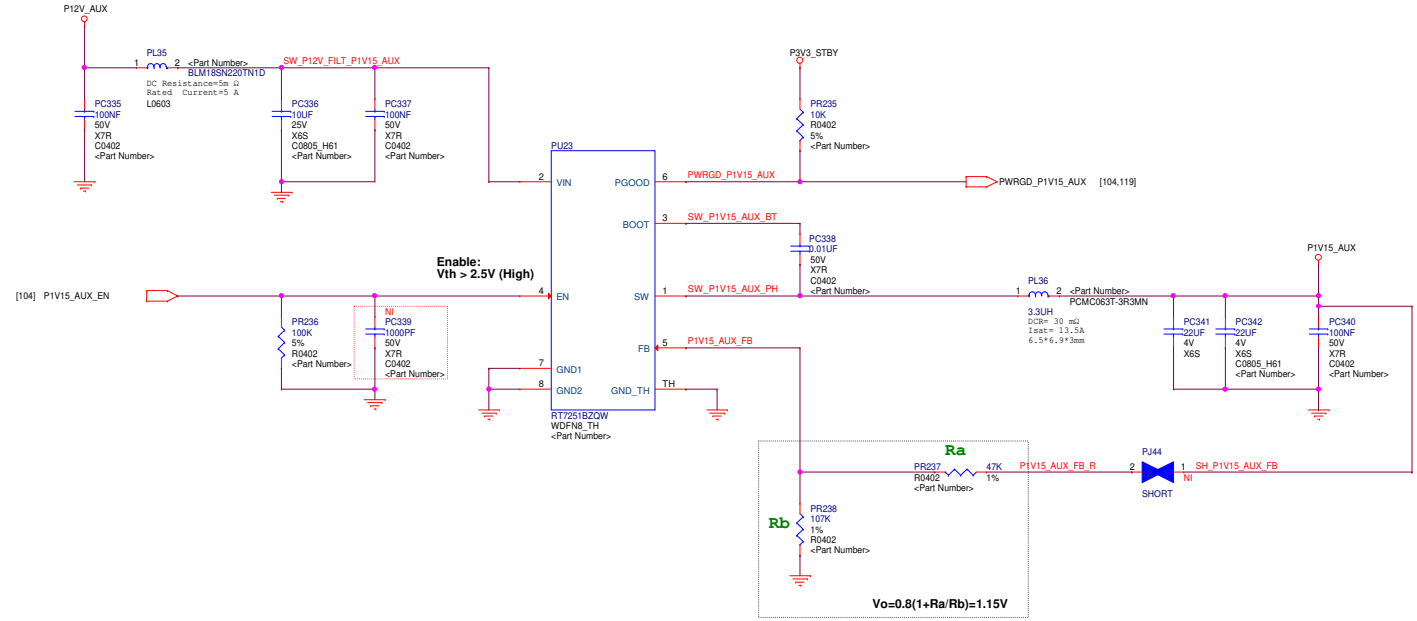


Design specification

Vout = 1.2V
Vout Ripple & Noise < 50mV (4.1%)
Vout Tolerance = +60 mV / -60 mV

Iout TDC = 0.56A
Iout MAX = 0.7A
Iout OCP = 2.8A (Spec)
Load Step = TBD
Slew Rate = 2.5A/us (TBD)

Fsw = 800k Hz (Fixed)
Efficiency > 90% @TDC
Current Mode Control



Design specification

Vout = 1.15 V
Vout Ripple & Noise < 50mV (4.3%)
Vout Tolerance = +57.5 mV / -57.5 mV

Iout TDC = 0.68A
Iout MAX = 0.78A
Iout OCP = 2.8A (Spec)
Load Step = TBD
Slew Rate = 2.5A/us (TBD)

Fsw = 800k Hz (Fixed)
Efficiency > 90% @TDC
Current Mode Control

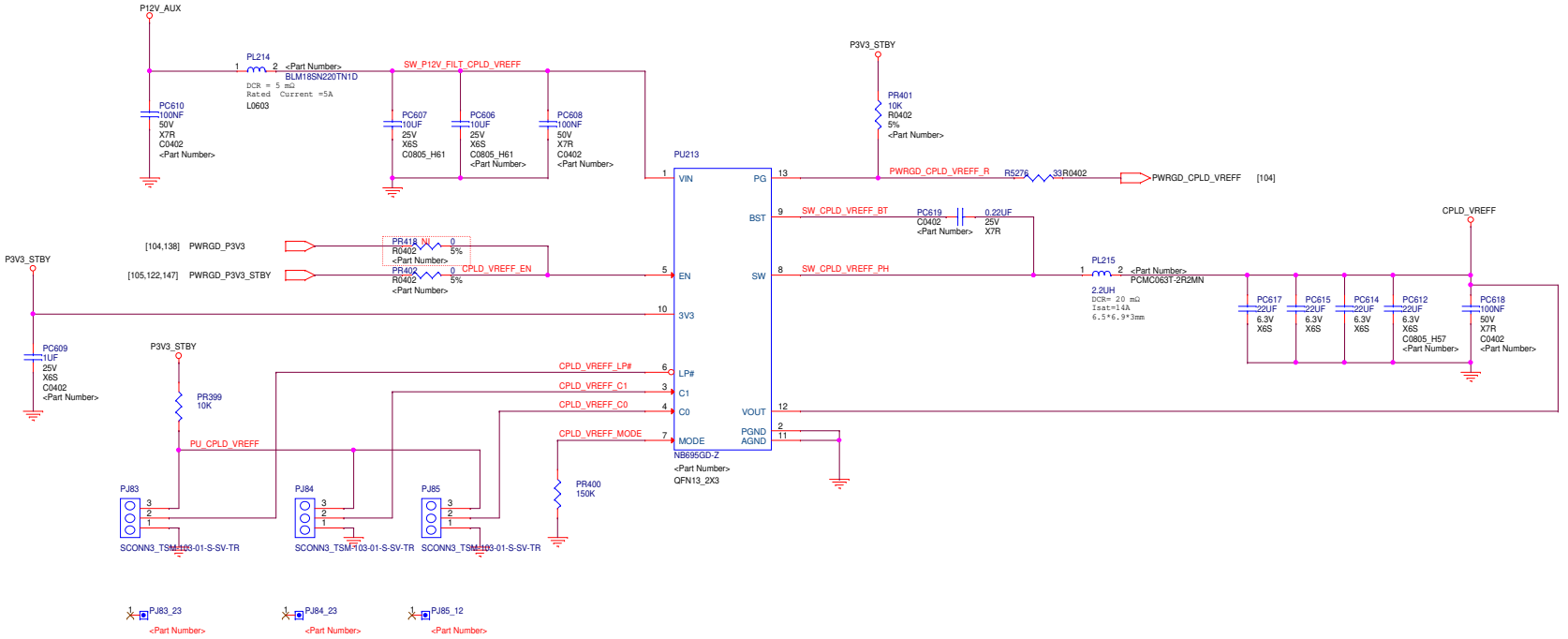
P1V2_AUX & P1V15_AUX

Design specification

Vout = 1.5 V,1.8V, 2.5V, 3.3V
Vout Ripple & Noise < 40mV
Vout Tolerance = +5% / -5%

Iout TDC = 1.12A
Iout MAX = 1.5A
Iout OCP = 3.0A (Spec)
Load Step = 0.6 (TBD)
Slew Rate = 2.5A/us (TBD)

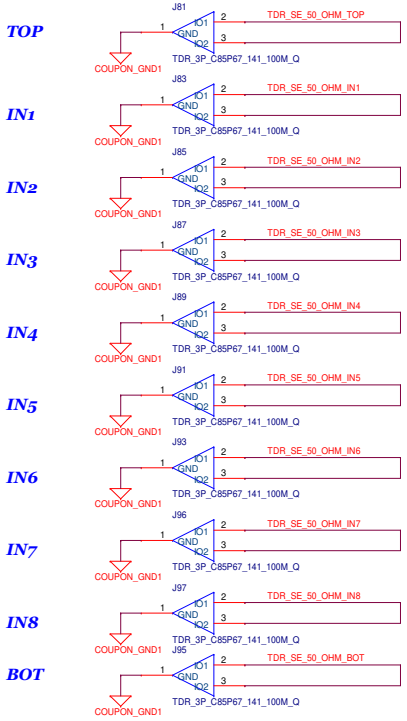
Fsw = 750k Hz
Efficiency > 90% @TDC
COT Control Mode



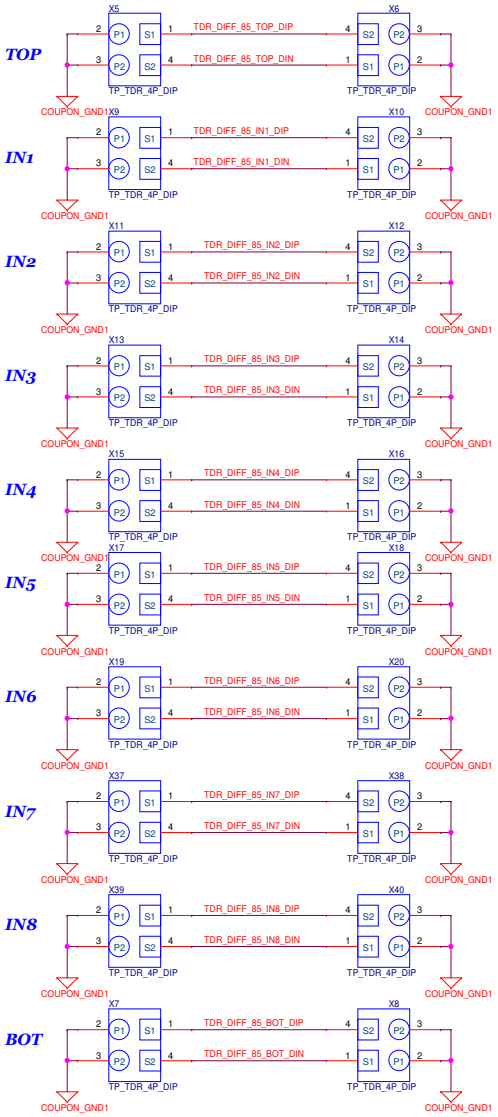
PJ83	PJ84	PJ85	VOUT(V)
1	0	0	1.2 V
1	0	1	1.5 V
1	1	0	1.8 V
1	1	1	2.5 V
0	1	1	3.3 V

VR_VREFF

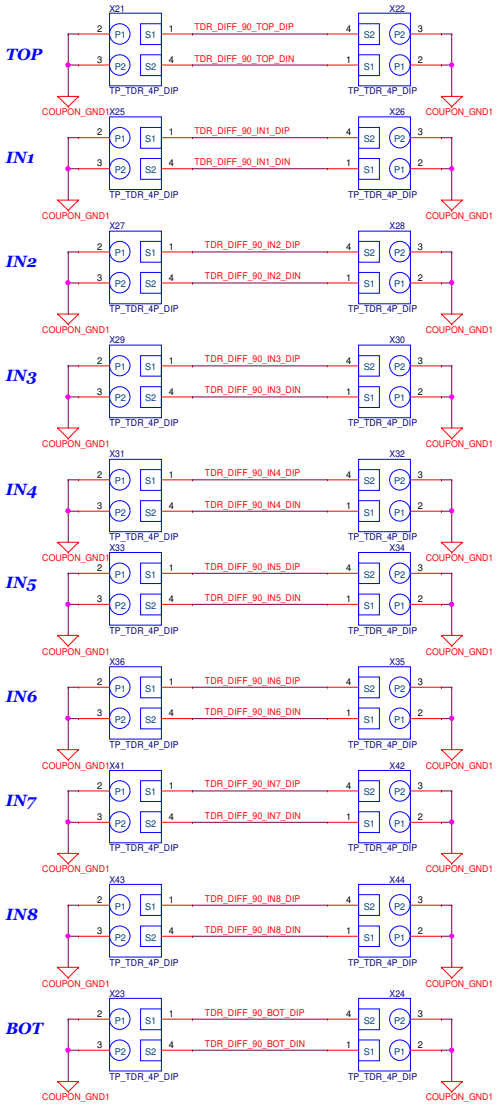
TDR-SINGLE



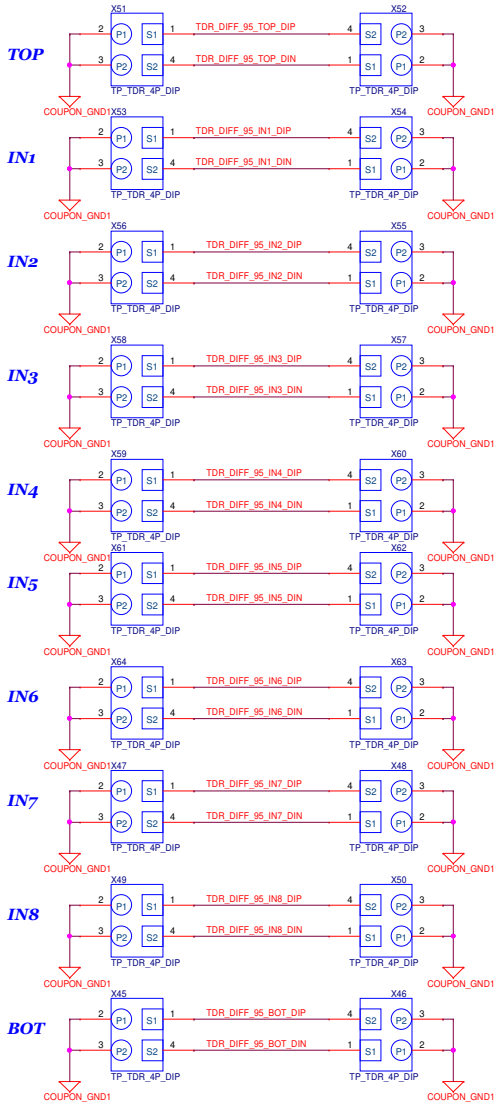
TDR-DIFFERENTIAL(85 ohm)



TDR-DIFFERENTIAL(90 ohm)



TDR-DIFFERENTIAL(95 ohm)



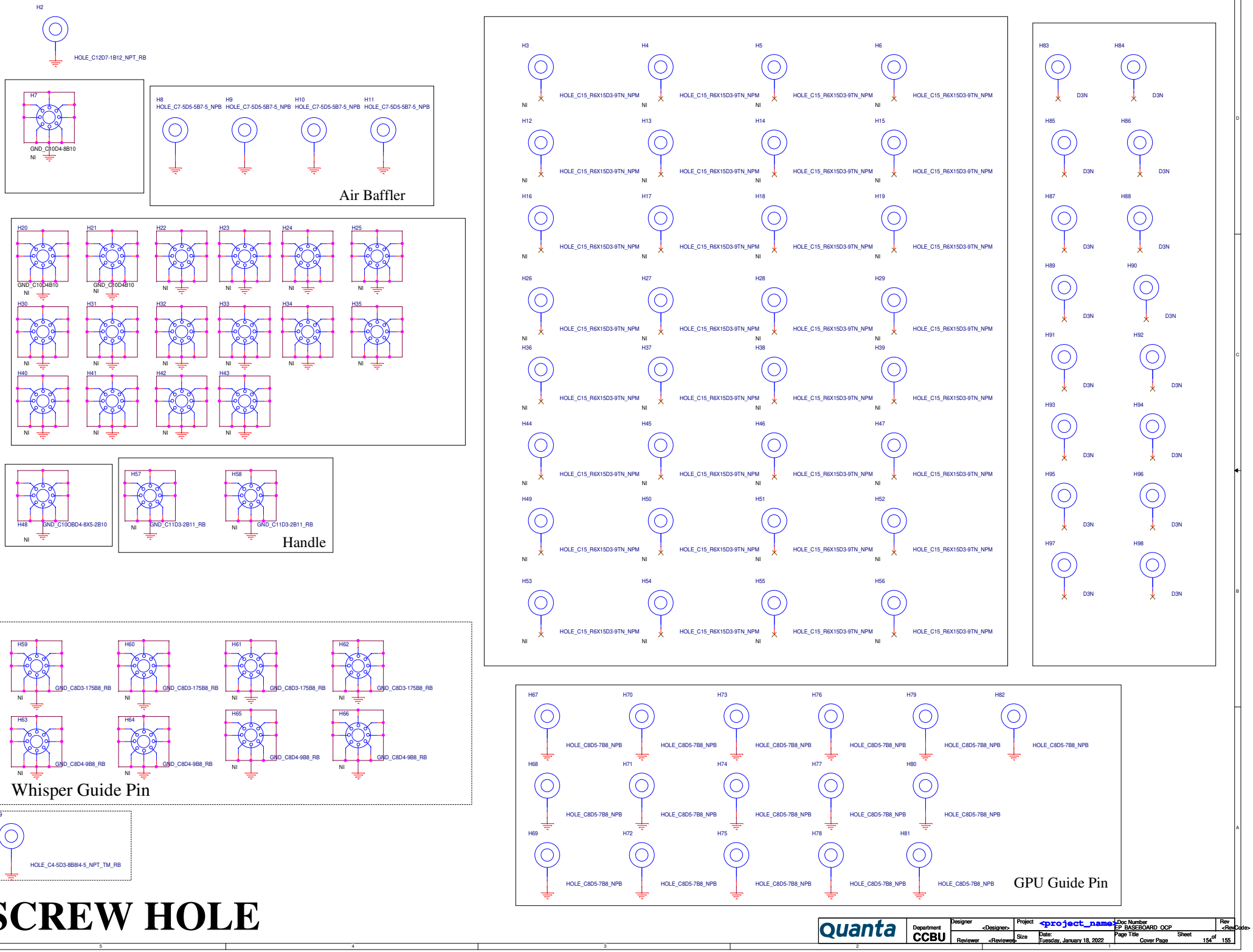
TDR



DELTA_L

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SCREW HOLE

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QUANTA_LOGO

QCT_LOGO

DM3

DUMMY_SYMBOL

QUANTA_LOGO_7X26

NI

WEEE

DM4

DUMMY_SYMBOL

WEEE

NI

PB-E1

DM5

DUMMY_SYMBOL

PB-E1_SMALL

NI

PCBA_LABEL

DM7

DUMMY_SYMBOL

PCBA_LABEL_15X5

NI

DM1

DUMMY_SYMBOL

PN+SN+MAC LABEL_27X6

<Part Number>

BIOS-BMCLABEL

DM6

DUMMY_SYMBOL

BIOS-BMCLABEL_10-5X10-5

NI

BARCODE

DM8

DUMMY_SYMBOL

BARCODE_20X6

NI

PCB_VENDER_LOGO

DM9

DUMMY_SYMBOL

PCB_VENDOR_LOGO_15X8

NI

BMC_FLASH

BIOS_FLASH

MECHANIC_SYMBOL

HEATSINK

U1_HS

DUMMY_SYMBOL

FBJG7002010

U20_HS

DUMMY_SYMBOL

FBJG7002010

U15_HS

DUMMY_SYMBOL

FBJG7002010

U17_HS

DUMMY_SYMBOL

FBJG7002010

BATTERY_SYMBOL

BT1_BAT

DUMMY_SYMBOL

AHL03002031

PICKUP_SYMBOL

PICKUP_SYMBOL

CBS_SYMBOL

TOOLING-HOLE_SYMBOL

DM10

DUMMY_SYMBOL

LASER_MARK_LABELS_10X10B

NI

DUMMY SYMBOL

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